Agilent E2960B Series

Hardware and Probing Guide

Agilent Technologies

Notices

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Safety Notices

CAUTION

A **CAUTION** notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a **CAUTION** notice until the indicated conditions are fully understood and met.

WARNING

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

Safety Summary

Safety Symbols on Instruments

Safety Symbol	Description
	Indicates warning or caution. If you see this symbol on a product, you must refer to the manuals for specific Warning or Caution information to avoid personal injury or damage to the product.
	Frame or chassis ground terminal. Typically connects to the equipment's metal frame.
	Indicates hazardous voltages and potential for electrical shock.
	Indicates that antistatic precautions should be taken.
	Indicates hot surface. Please do not touch.
	Indicates laser radiation turned on.
	CSA is the Canadian certification mark to demonstrate compliance with the Safety requirements.
	CE compliance marking to the EU Safety and EMC Directives. ISM GRP-1A classification according to the international EMC standard. ICES/NMB-001 compliance marking to the Canadian EMC standard.

General Safety Precautions

The following general safety precautions must be observed during all phases of operation of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument.

Agilent Technologies Inc. assumes no liability for the customer's failure to comply with these requirements.

Before operation, review the instrument and manual for safety markings and instructions. You must follow these to ensure safe operation and to maintain the instrument in safe condition.

General

This product is a Safety Class 1 instrument (provided with a protective earth terminal). The protective features of this product may be impaired if it is used in a manner not specified in the operation instructions.

All Light Emitting Diodes (LEDs) used in this product are Class 1 LEDs as per IEC 60825-1.

Environment Conditions

This instrument is intended for indoor use in an installation category II, pollution degree 2 environment. It is designed to operate at a maximum relative humidity of 95% and at altitudes of up to 2000 meters.

Refer to the specifications tables for the ac mains voltage requirements and ambient operating temperature range.

Before Applying Power

Verify that all safety precautions are taken. The power cable inlet of the instrument serves as a device to disconnect from the mains in case of hazard. The instrument must be positioned so that the operator can easily access the power cable inlet. When the instrument is rack mounted the rack must be provided with an easily accessible mains switch.

Ground the Instrument

To minimize shock hazard, the instrument chassis and cover must be connected to an electrical protective earth ground. The instrument must be connected to the ac power mains through a grounded power cable, with the ground wire firmly connected to an electrical ground (safety ground) at the power outlet. Any interruption of the protective (grounding) conductor or disconnection of the protective earth terminal will cause a potential shock hazard that could result in personal injury.

Do Not Operate in an Explosive Atmosphere

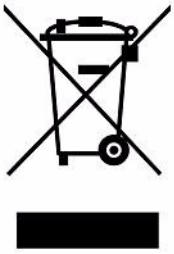
Do not operate the instrument in the presence of flammable gases or fumes.

Do Not Remove the Instrument Cover

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made only by qualified personnel.

Instruments that appear damaged or defective should be made inoperative and secured against unintended operation until they can be repaired by qualified service personnel.

Environmental Information



This product complies with the WEEE Directive (2002/96/EC) marking requirements. The affixed label indicates that you must not discard this electrical/ electronic product in domestic household waste.

Product Category: With reference to the equipment types in the WEEE Directive Annex I, this product is classed as a "Monitoring and Control instrumentation" product.

Do not dispose in domestic household waste.

To return unwanted products, contact your local Agilent office, or see www.agilent.com/environment/product/ for more information.

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1 N5306A I/O Module

This chapter provides information on the N5306A I/O module used for PCIe.

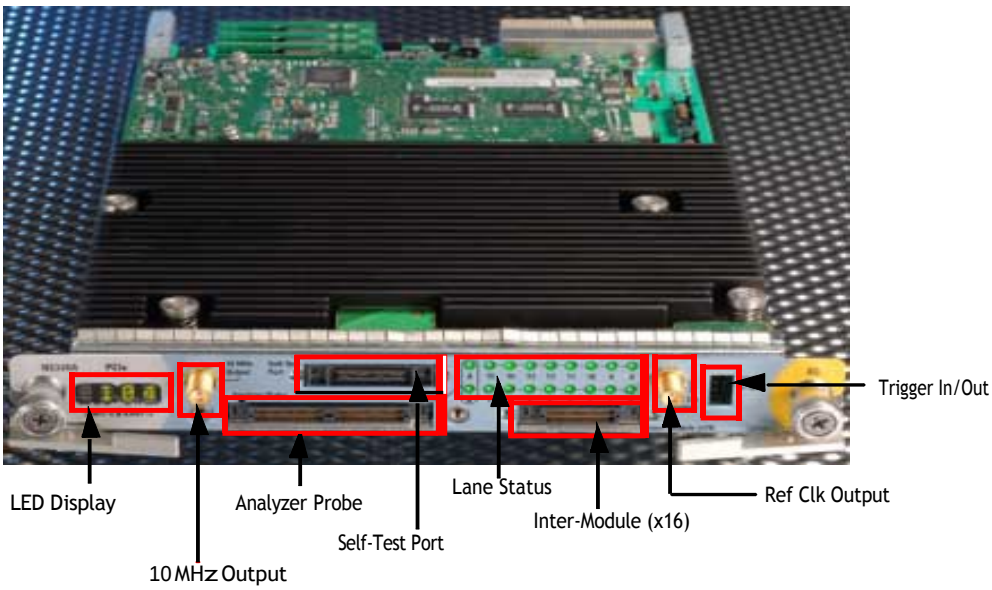


Figure 1 N5306A I/O Module

As shown in Figure 1, the N5306A I/O module has the following components:

- **LED Display**— This component is used to display the diagnostic information when fatal faults are discovered, and to indicate progress during the bootstrap. If everything is working properly, then this component displays the module number, such as 103.
- **10 MHz Output**— This component is a reference clock, which is used for generating timestamps in Protocol Analyzer. This component delievers 10 MHz output.
- **Analyzer Probe**— This component is used to connect the midbus probe *module connector* with N5306A and N5307A (slot interposer card).

  For complete information on midbus probe, refer to *Agilent Soft Touch Midbus Probe, User's Guide*.

For information on plugging midbus probe module connector with N5306A Analyzer Probe, refer to *Agilent System Protocol Tester, Installation Guide*.

- **Self-Test Port**— This component is a loopback board, and is used to connect the midbus probe *tip* with N5306A. The one side of this loopback board has a retainer for the probe, and the other side has the connector for the self-test port. To verify if N5306A I/O module and midbus probe are working properly, plug in this loopback board into the self-test port and then watch the lane status.
- **Lane Status**— This component has 18 LED bullets that displays the status of the lane by using different colored bullets. Two bullets, labelled **A** and **B**, indicate global status information. Different colors used to indicate global status information are:
  - **Grey** — This colored bullet means system is not configured.
  - **Red** — This colored bullet means the speed is not detected or the system is not configured.
  - **Yellow** — This colored bullet represents speed of 2.5 Gb/s
  - **Green** — This colored bullet represents speed of 5 Gb/s.

  Other 16 LED bullets, labelled **0** to **15**, indicate the status of each lane. These bullets are:
  - **Red** — This colored bullets means that there are no signals or the lane is electrically idle.
  - **Orange** — This colored bullet marks the presence of invalid signals on the lane.
  - **Green** — This colored bullet means that the data on the lane is deskewed.
  - **Blinking Green** — This colored bullet means that the data on the lane is skewed. It corresponds to *yellow* in the Port Overview pane in the Protocol Analyzer GUI.
  - **Grey** — This colored bullet means that the lane is not configured. For example, if you are using x4 link width, then first four bullets of the lane would be green and rest of the bullets would be grey colored bullets.
- **Inter- Module (x16)**— This component is used to share information with another N5306A I/O module in the same chassis. The features of this component are not yet supported by the System Protocol Tester platform.
- **Ref Clk Output**— This components is a *reference clock*, which N5306A use to process the data internally. This components delivers 100 MHz output.
- **Trigger In/Out**— This component is used to listen to external trigger in from a different device or send external trigger out to another device.

The following figure shows meaning of the pins of the Trigger In/Out component.

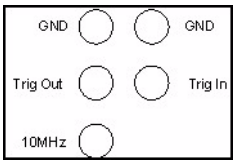


Figure 2 Trigger In/Out Pins

The following are some important points about the Trigger In/Out component:

- The outputs circuitry is designed to work into open in order to fit to the LA input that is typically in the K-ohms range.
- Maximum trigger input voltage should not exceed 3.3 V.
- Trigger Out and 10 MHz Out have nominal output level of 2.0 V after 20 ns minimum pulse width.
- Minimum Trigger In duration is ~20 ns.

NOTE Use *trigger cable* to send or receive external trigger in and out events.

WARNING **Do not directly touch any component on the I/O module. It may be hot.**

CAUTION Components on the I/O module are sensitive to the static electricity. Therefore, take necessary anti-static precautions, such as wear a grounded wrist strap, to minimize the possibility of electrostatic damage.

1 N5306A I/O Module

2 N5322A Extended Interface Module

This chapter provides information on the N5322A extended interface module used for PCIe.

The N5322A extended interface module is used with the N5306A module to capture the traffic of DUTs that use PCIe power management (L0s, L1, L2/L3).

The following figure shows the N5322A extended interface module.

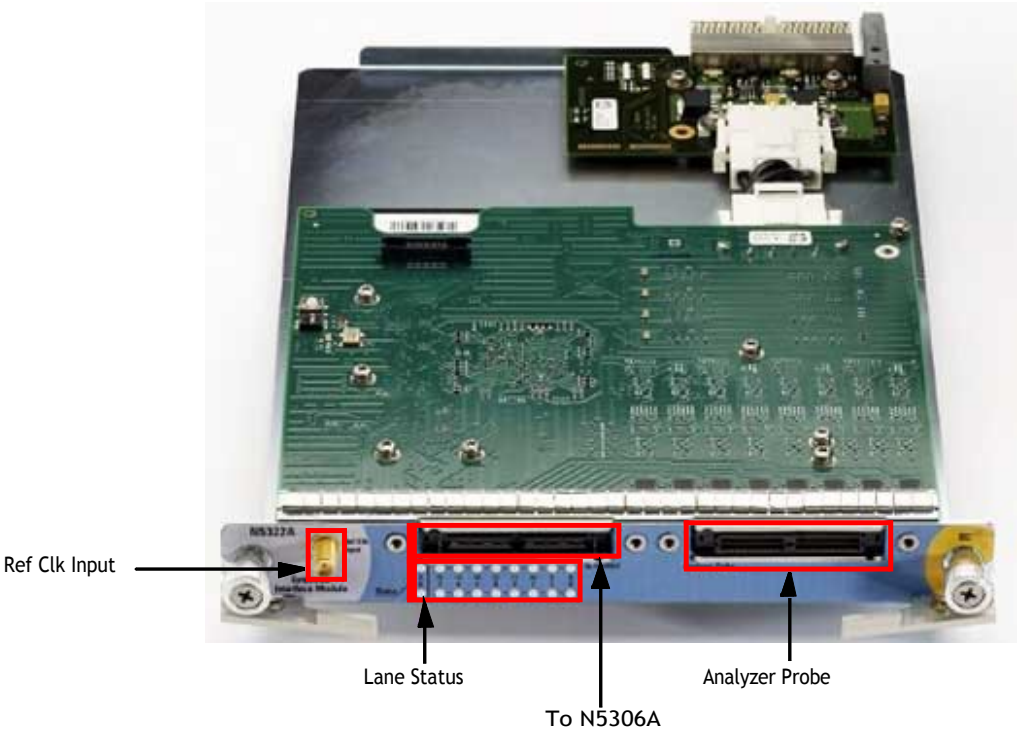


Figure 3 N5322A Extended Interface Module

As shown in the above figure, the N5322A module has the following components:

- **Ref Clk Input**— This component is used as an alternate 100 MHz reference clock input.

- **Analyzer Probe**— This component is used to connect the N5322A module with the following probe types:
  - N4241A Straight
  - N4242A Swizzled
  - N4243A Split Cable
  - N5315A Solid Slot Interposer
  - N5317A PCIe Gen1 Probe Connection Cable
  - N4241F Flying Leads
- **To N5306A**— This component is used to connect N5322A with N5306A using the Extended Interface Module interconnect cable.

  The following figure shows how you can use N5322A and N5306A modules, and a probe type together.

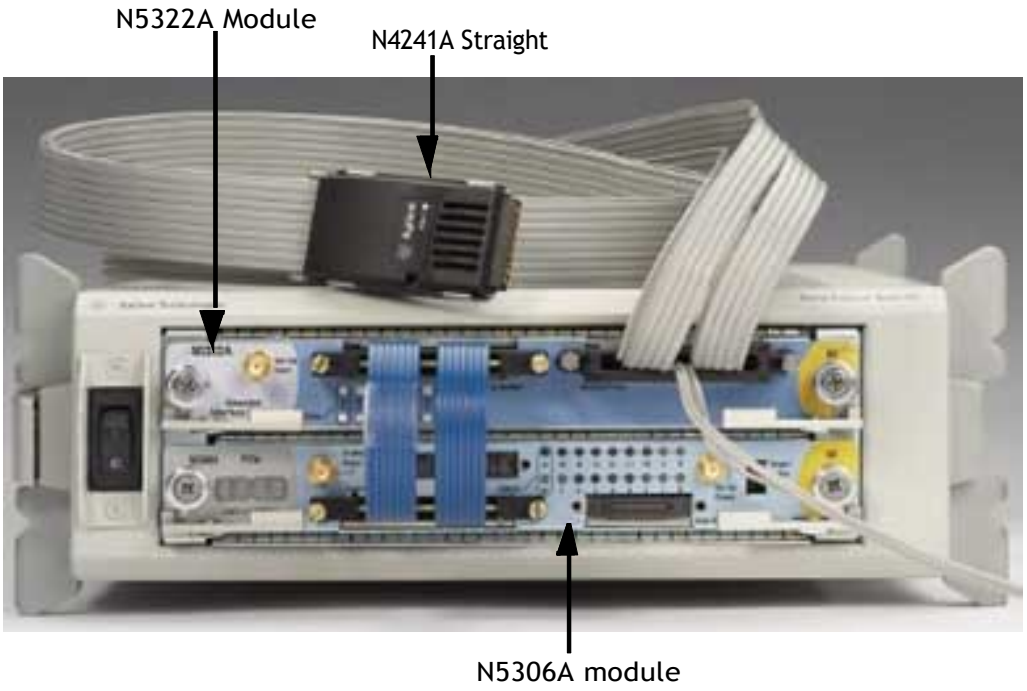


Figure 4 N5322A paired with N5306A

NOTE

N5322A and N5306A modules should be used as a pair. That is:

- Use 1 N5306A and 1 N5322A for a x8 setup.
- Use 2 N5306A and 2 N5322A for a x16 setup.

- **Lane Status**— This component has 18 LEDs that display the status of the lane by using different colors. Two LEDs, labelled **A** and **B**, indicate global status information. Different colors used to indicate global status information are:
  - **Green** — This colored LED means that N5322A and N5306A modules are connected, the Port Overview pane in Protocol Analyzer is showing *Connected*, and also the check box for N5322A in the Hardware Setup dialog box is *selected*.
  - **Yellow** — This colored LED means that N5322A and N5306A modules are connected, the Port Overview pane in Protocol Analyzer is also showing *Connected*, but the check box for N5322A in the Hardware Setup dialog box is *not selected*.
  - **Red** — This colored LED means that N5322A is not connected with N5306A.

  Other 16 LEDs, labelled **0** to **15**, indicate the status of each lane. These LEDs are:
  - **Green** — This colored LED means that the lane is not in electrical idle state.
  - **Grey** — This colored LED means that the lane is not configured. For example, if you are using x4 link width, then first four bullets of the lane would be green and rest of the bullets would be grey colored bullets.
  - **Red** — This colored LED means there are no signals or the lane is electrically idle.

WARNING **Do not directly touch any component on the N5322A module. It may be hot.**

CAUTION Components on the N5322A module are sensitive to the static electricity. Therefore, take necessary anti-static precautions, such as wear a grounded wrist strap, to minimize the possibility of electrostatic damage.

3 N5309A Exerciser Card and Extension Card

N5309A Exerciser Card 16
N5309-66417 Exerciser Extension Card 20

This chapter provides information on the N5309A exerciser card and the N5309-66417 exerciser extension card used for PCIe.

N5309A Exerciser Card

The following figure displays the N5309A exerciser card.

Figure 5 N5309A Exerciser Card

Components of the N5309A exerciser card are described below:

- **Ref Clk Input**— This component can be used as an alternative 100 MHz reference clock input.
- **LED Display**— This component displays the module number, such as *module number 10003*, to which N5309A is configured. The module number displayed here scrolls horizontally from right to left.
- **Status LEDs (on board)**— This component has the following LEDs to display the status information.

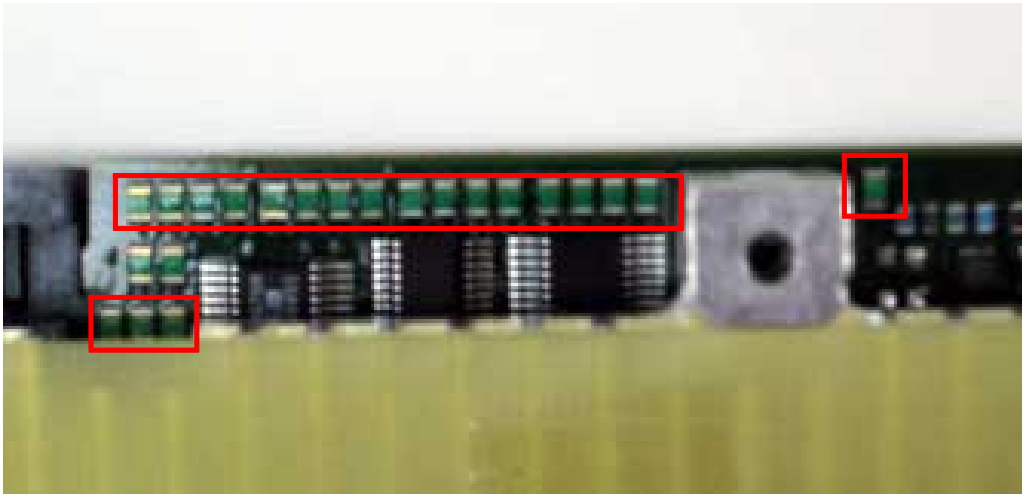


Figure 6 N5309A Exerciser card - Status LEDs

- First 16 LEDs displays the status of the link.
- One LED, separately highlighted on the right, shows the power status of the board.
- Last three LEDs shows the power status of DUT.

- **Edge Connector**— This component is used to connect N5308A with a PCIe Connector on the backplane board, or with a system.
- **Trigger Connector**— This component is a six-pin header, and is used to connect the trigger cable (N5306-61604) to enable triggering between Protocol Exerciser and Protocol Analyzer. In this scenario, the other end of the trigger cable is plugged into the trigger connector of the Protocol Analyzer module.

  You can also use this connector for cross-triggering with other instruments, such as Logic Analyzer.

  The following figure shows the meaning of the pins in the Trigger Connector component:

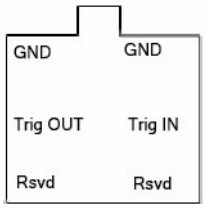


Figure 7 Trigger Connector Pins

- **Power Supply Connector**— This component is used to connect N5309A with the external power supply.

  Use the power supply delivered with N5309A only.

- **Status LED (on front bracket)**— This LED represents the following different states:
  - *No light* state means there is no link up.
  - *Green light* means there is a link up at the Gen2 speed.
  - *Blinking green light* means there is a link up at the Gen1 speed.
- **USB Connector**— This component is used to connect N5309A with the controller PC using the USB cable.

  The following figure shows the Trigger Connector, Power Supply Connector, Link Status LED, and USB Connector components.

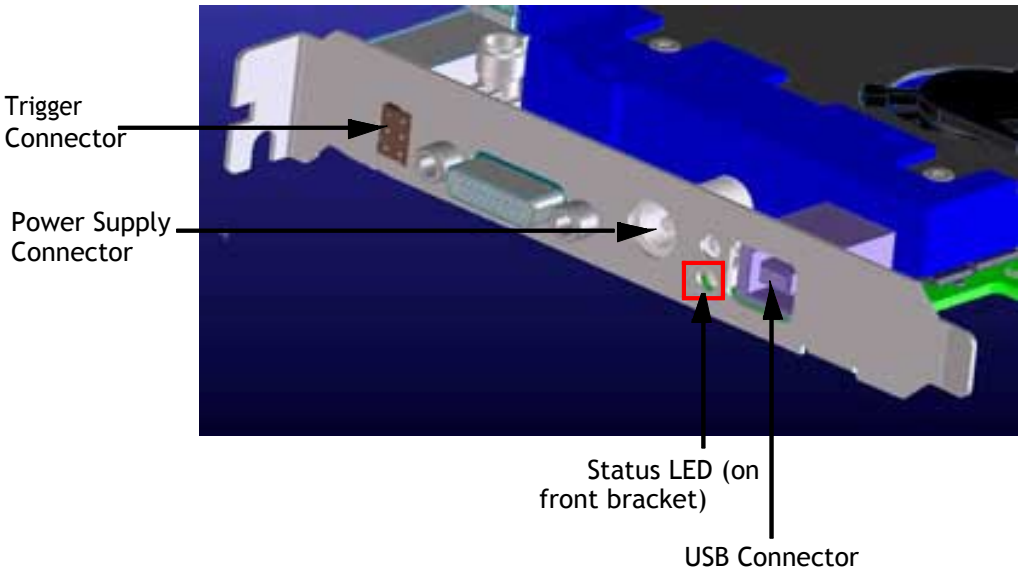


Figure 8 N5309A Exerciser Card

NOTE

The N5309A exerciser card also has the Extension Card Connector component at its top, which is used to connect the Exerciser Extension Card with N5309A. For more information on this component and exerciser extension card, refer to "N5309-66417 Exerciser Extension Card" on page 20.

For more information on the N5309A exerciser card, refer to:

- *Agilent Protocol Exerciser, User's Guide*

WARNING **Do not directly touch any component on the N5309A exerciser card. It may be hot.**

CAUTION Components on the N5309A exerciser card are sensitive to the static electricity. Therefore, take necessary anti-static precautions, such as wear a grounded wrist strap, to minimize the possibility of electrostatic damage.

N5309-66417 Exerciser Extension Card

This chapter provides information on the N5309-66417 exerciser extension card used with the N5309A exerciser card for PCIe.

The following figure displays the N5309-66417 exerciser extension card.

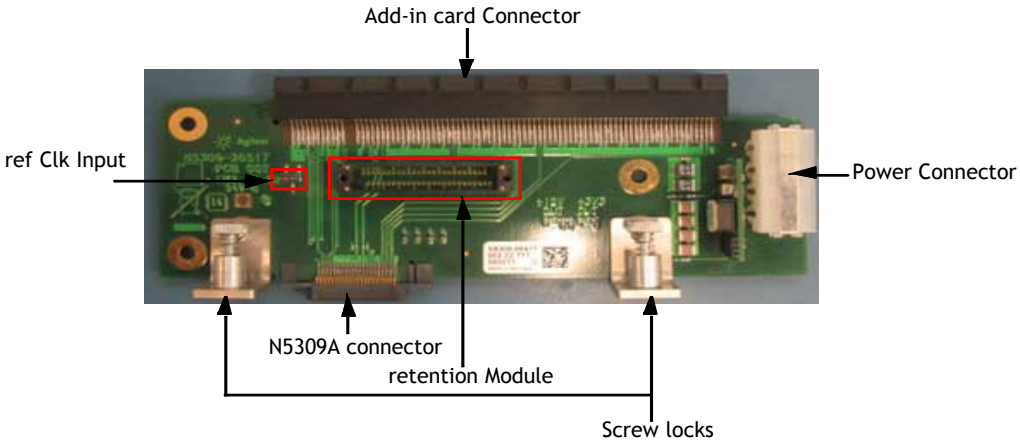


Figure 9 N5309-66417 Exerciser Extension Card

Components of the N5309-66417 exerciser extension card are described below:

- **Ref Clk Input**— This component can be used as an alternative 100 MHz reference clock input.
- **Add-in Card Connector**— This component is used to connect any add-in PCIe card at the top of N5309-66417.
- **Retention Module**— This component is used to connect the midbus probe, which is then used for capturing traffic between the N5309A exerciser card and the add-in card.
- **Power Connector**— This component is used to provide power supply to an add-in card, which is hooked on the N5309-66417 card.
- **N5309A Connector**— This component is used to connect the N5309-66417 card with the N5309A exerciser card.

  To connect the two cards:

  a Insert the N5309A Connector component into the *Extension Card Connector* component of the N5309A card.

  b Tighten the *screw locks* of the N5309-66417 card to tightly align it with the N5309A card.

The following figure shows the N5309-66417 card connected with the N5309A card.

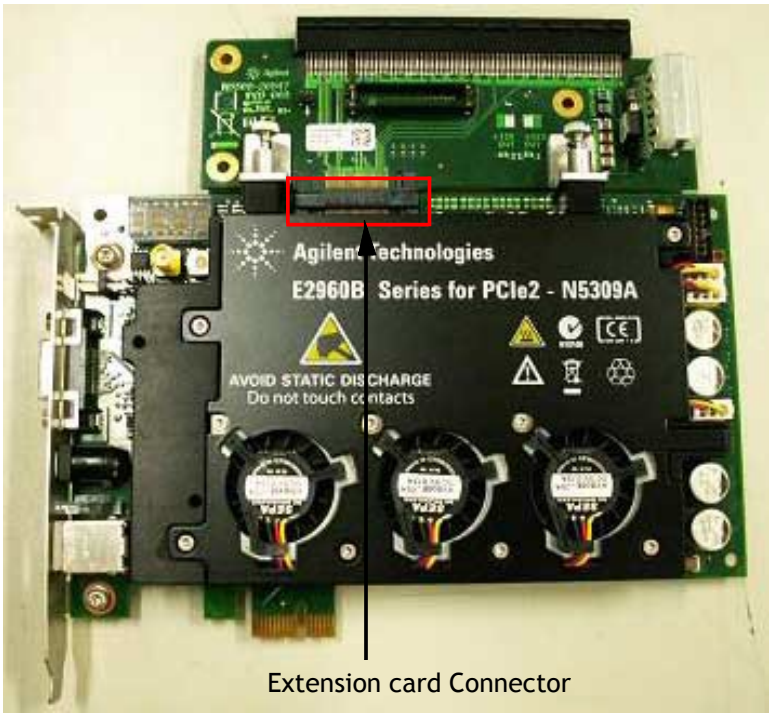


Figure 10 N5309-66417 connected with N5309A

NOTE The N5309-66417 exerciser extension card supports linkup only on the x1 link width.

WARNING **Do not directly touch any component on the N5309-66417 exerciser extension card. It may be hot.**

CAUTION Components on the N5309-66417 exerciser extension card are sensitive to the static electricity. Therefore, take necessary anti-static precautions, such as wear a grounded wrist strap, to minimize the possibility of electrostatic damage.

3 N5309A Exerciser Card and Extension Card

4 N5323A Jammer Card

This chapter provides information on the N5323A jammer card used for PCIe.

The following figure displays the N5323A Jammer card.

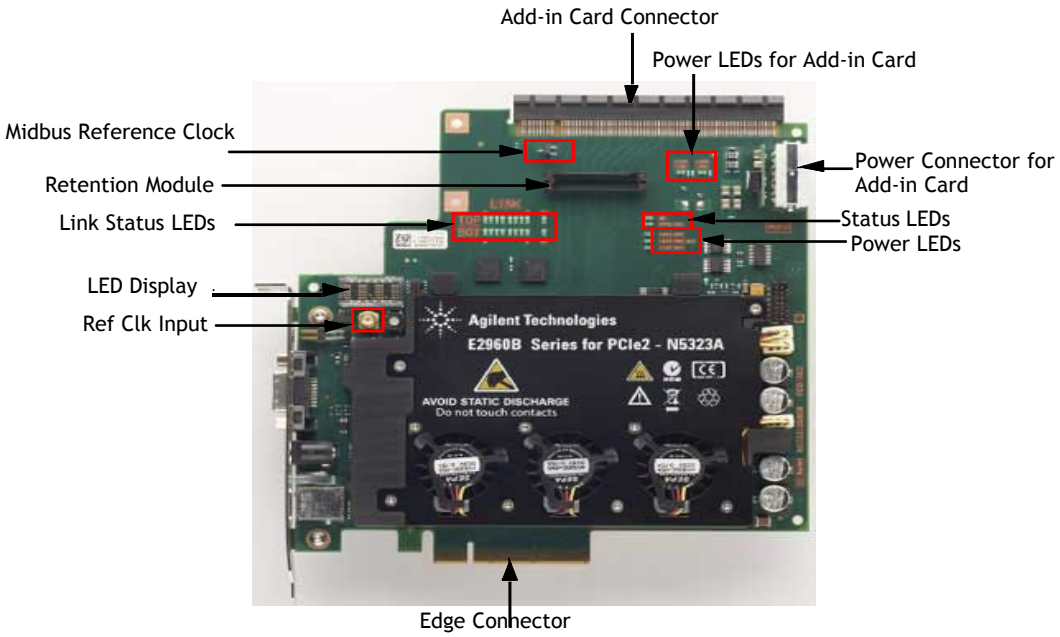


Figure 11 N5323A Jammer Card

Components of the N5323A jammer card are described below:

- **Ref Clk Input**— This component can be used as an alternative 100 MHz reference clock input.
- **LED Display**— This component displays the following messages:
  - *Module number* (such as module number 10003) to which N5323A is configured. The module number displayed here scrolls horizontally from right to left.
  - *Serial number* of the board, when you open the **Update GUI** tool from **Start > Programs > Agilent N2X > PCIE Jammer 71. Release**.

- *FPPR* when the firmware is being programmed.
- *FWPR* when the firmware is programmed, and the board requires a power cycle.

- **Retention Module**— This component is used to connect the midbus probe to the N5323A jammer card, which allows midbus probe to be used for capturing traffic between N5323A and the add-in card.

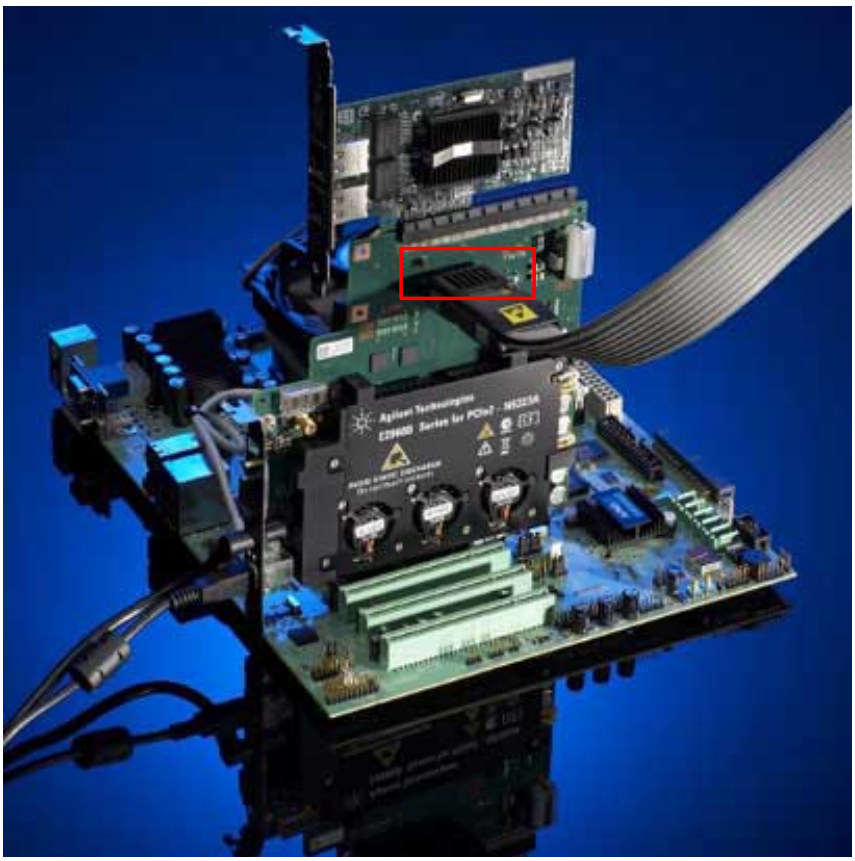


Figure 12 Midbus probe plugged into the retention module

- **Midbus Reference Clock**— This component can be used to connect the reference clock to the midbus probe.

NOTE

For information on midbus probe, refer to *Agilent Soft Touch Midbus Probe, User's Guide* and *Agilent System Protocol Tester, Installation Guide*.

- **Power Connector for add-in card**— This component is used to provide power supply to the add-in card, which is hooked on the N5323A jammer card.

- **Power LEDs for Add- in Card**— This component has two LEDs marked as *+3V3 TOP* and *+12V TOP* displaying the status of the PCIe power to the add-in card.
- **Edge Connector**— This component is used to connect N5323A with a PCIe Connector on the backplane board, or with a system.
- **Add-in Card Connector**— This component is used to connect any add-in PCIe card at the top of N5323A.
- **Link Status LEDs**— This component has the following LEDs to display the PCIe link status information.

  The upper row (labeled TOP) displays the status of the *link to add-in-card*, and the lower row (labelled *BOT*) displays the status of the *link to system* or *backplane*.

  The link status LEDs (labelled ST) represent the following states:

  - *No light* state means there is no link up.
  - *Green light* means there is a link up at the Gen2 speed.
  - *Blinking green light* means there is a link up at the Gen1 speed.
- **Status LEDs**— This component has two LEDs marked as *HB* and *FPGA RDY* displaying the status of the board.

  Flashing HB LED shows that the micro controller is running, and FPGA RDY shows that the FPGA image is loaded and ready.
- **Power LEDs**— This component has three LEDs marked as *+3V3 BOT*, *+3V3 BOT AUX*, and *+12V BOT* displaying the status of the PCIe power supplies from the system or backplane.
- **Trigger Connector**— This component is a six-pin header, and is used to connect the trigger cable (N5306-61604) to enable triggering between Jammer and Protocol Analyzer. In this scenario, the other end of the trigger cable is plugged into the trigger connector of the Protocol Analyzer module.

  You can also use this connector for cross-triggering with other instruments, such as Logic Analyzer.

  The following figure shows the meaning of the pins in the Trigger Connector component:

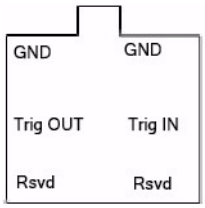


Figure 13 Trigger Connector Pins

- **Power Supply Connector**— This component is used to connect N5323A with the external power supply.

  Use the power supply delivered with N5323A only.

- **USB Connector**— This component is used to connect N5323A with the controller PC using the USB cable.

The following figure shows the Trigger Connector, Power Supply Connector, Link Status LED, and USB Connector components.

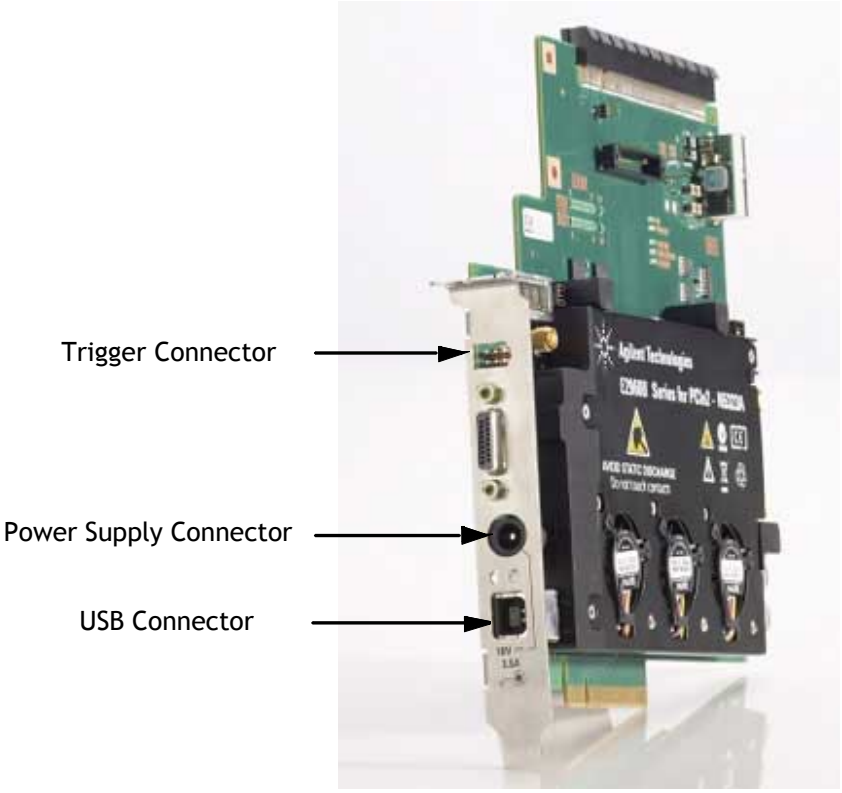


Figure 14 N5323A Jammer Card

WARNING **Do not directly touch any component on the N5323A jammer card. It may be hot.**

CAUTION Components on the N5323A jammer card are sensitive to the static electricity. Therefore, take necessary anti-static precautions, such as wear a grounded wrist strap, to minimize the possibility of electrostatic damage.

5 N5315 Solid Slot Interposer Card

This chapter provides information on the N5315 solid slot interposer card used for PCIe.

The *N5315 solid slot interposer* card comes in four form factors: x1, x4, x8 and x16 link width.

The following figure shows the N5315 solid slot interposer card for the x16 link width.

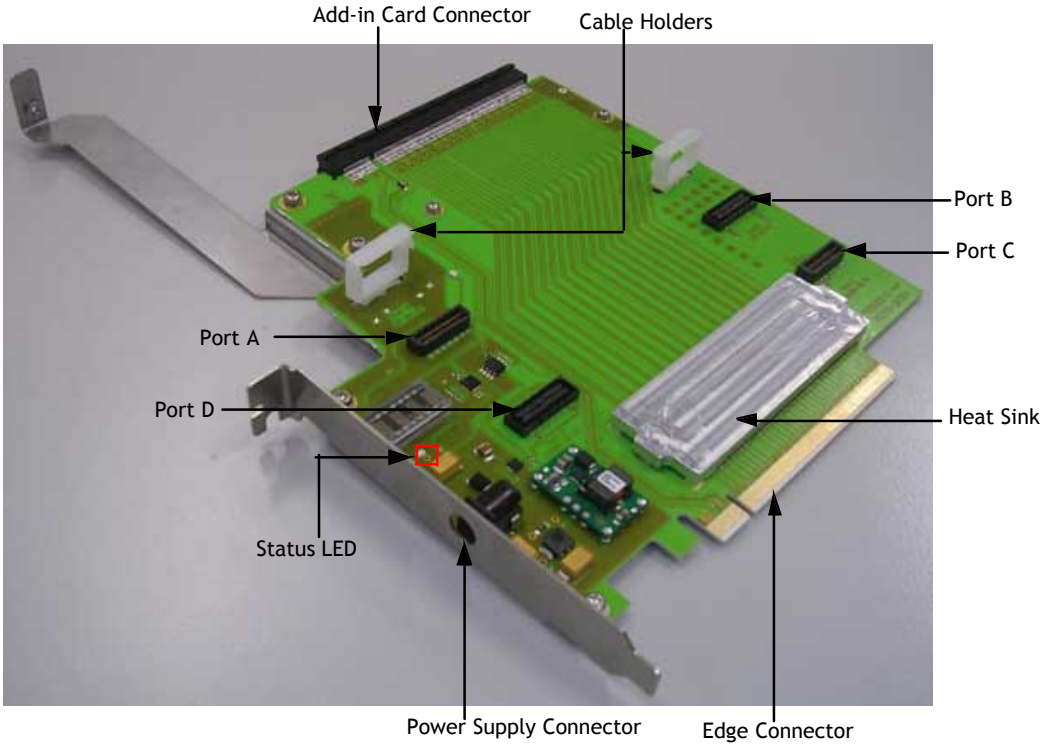


Figure 15 N5315 Solid Slot Interposer Card

Components shown in the above figure are described below:

- **Add-in Card Connector**— This component is used to connect any add-in PCIe card at the top of N5315.

- **Edge Connector**— This component is used to connect N5315 with a PCIe Connector on the backplane board, or with a system.

  This component comes with a protective foam cover to protect it from electrostatic damage.

Figure 16 Protective Foam Cover for Edge Connector

NOTE

Please remove the protective foam cover before using the card, and attach it again when the card is not in use.

- **Ports**— N5315 has the following ports:
  - **Port A** — This port is for lanes 0-7, downstream.
  - **Port B** — This port is for lanes 8-15, downstream.
  - **Port C** — This port is for lanes 8-15, upstream.
  - **Port D** — This port is for lanes 0-7, upstream.

  If you use N5315 for x8 link width, then Port B and C will not be available.
- **Cable Holders**— These components hold the *N5315-61601 Solid Slot Interposer* cables that connect the N5306A I/O module to the N5315 card.

  The following figure shows the N5315-61601 cable.

Figure 17 N5315-61601 Solid Slot Interposer cable

To use this cable, plug its *Module Connector* in the *Analyzer Probe* component of the N5306A I/O module, and plug its *port connectors* in the ports of the N5315 card.

For example, a x8 setup requires one N5315-61601 cable, whereas a x16 setup requires two N5315-61601 cables.

For a x8 setup, plug the port connectors of the N5315-61601 cable into port A and D of the N5315 card, and its module connector into the Analyzer Probe component of the N5306A I/O module.

For a x16 setup, plug the port connectors of the one N5315-61601 cable into the A and D ports, and the port connectors of the second cable into the B and C ports. After this, plug the module connectors of these two cables into the Analyzer Probe components of the two N5306A I/O modules.

The following figure shows the two N5315-61601 cables connected to the ports and supported by the cable holders.

Figure 18 N5315 with Cables

- **Status LED**— This component indicates whether the N5315 card is powered. It has the following two states:
  - *No light* state means the card is not powered.
  - *Green light* means the card is powered.
- **Heat Sink**— This component absorbs and dissipates heat of the card.
- **Power Supply Connector**— This component is used to connect N5315 with the external power supply.

  Use the power supply delivered with N5315 only.

NOTE

Power supply specifications are:

Input: 100-240 V~, 47-63 Hz 130-160 VA 1.5 A MAX

DC Output: +18 ⎓ 3.6 A 63 W MAX

WARNING

Do not directly touch any component on the N5315 solid slot interposer card. It may be hot.

CAUTION

Components on the N5315 solid slot interposer card are sensitive to the static electricity. Therefore, take necessary anti-static precautions, such as wear a grounded wrist strap, to minimize the possibility of electrostatic damage.

6 N5316A Backplane Board for PCIe

This chapter provides information on the N5316A test backplane board used for PCIe 5 Gb/s.

The following figures show the N5316A test backplane board for PCIe 5 Gb/s.

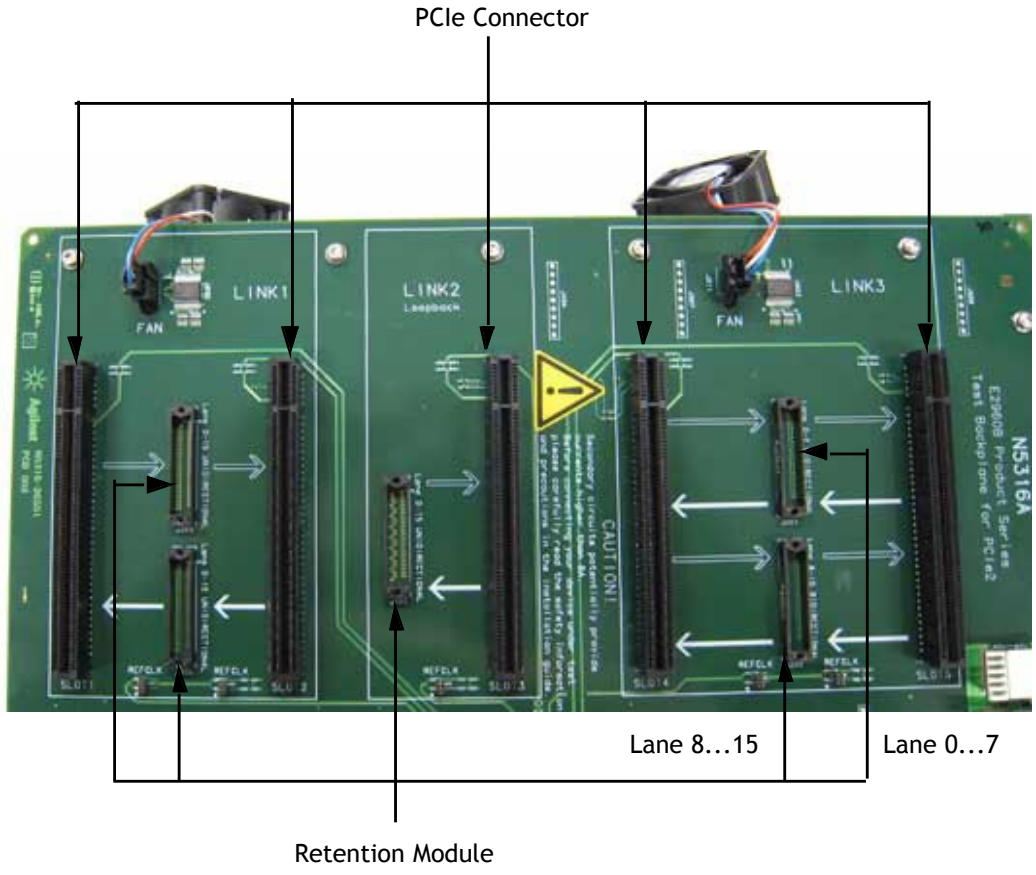


Figure 19 N5316A Backplane Board

As shown in the previous figure, the N5316A backplane board has:

- Five *retention modules* for midbus probe.

- Five *PCIe connectors* for the slot interposer cards, exerciser cards, and other add- in cards (like LAN or graphic card).

  As shown on the backplane board, arrows between the retention modules and PCIe connectors show the direction in which the traffic flows.

  All these retention modules and PCIe connectors are arranged inside the following three sections:

  - **LINK1**— The retention modules in this section are unidirectional and can support link width upto x16. One direction of lanes 0...15 is routed to each retention module supporting upto x16. Using N4241A midbus probe here will display only upstreams or downstreams lanes on the I/O module. To view lanes in both directions, use the N4242A midbus probe.
  - **LINK2**— The retention module and PCIe connector in this section is used for loopback, wherein one PCIe card transmits packets as well as receives its own transmitted packets. Here, the midbus probe in the retention module captures the traffic flowing through loopback.
  - **LINK3**— The retention modules in this section are bidirectional and can support upto x8 link width. Both directions of lanes 0...7 are routed to one retention module, and lanes 8...15 to the other. Using a N4241A midbus probe, you can capture upto x8 link width on one retention module.

NOTE Lanes and directions are printed on the N5316A backplane board as well.

The main application of this board is in testing an add- in card, such as a LAN or graphic card, using an exerciser card and a midbus probe. In this case, you plug the exerciser card into one PCIe connector and the add- in card into the other PCIe connector. Then, you plug the midbus probe into one of the retention module between the add- in and exerciser cards. This enables you to capture and analyze the traffic flowing between the add- in and exerciser cards.

- Five *REFCLK connectors* (reference clock connector), one for each PCIe connector. You use these connectors when you want to supply external clock feed to the PCIe connectors. In this situation, you use the Y-cable, whose tail is plugged into the external clock source and two heads into the two REFCLK connectors.
- Two *fan connectors* for the exhausts that you can use to keep the temperature of the board under control.

NOTE For information on midbus probe, refer to *Agilent Midbus 2.0, User's Guide* and *Agilent System Protocol Tester, Installation Guide*.

NOTE For information on setting up the metal sheet and exerciser card, refer to *Agilent System Protocol Tester, Installation Guide*.

The following figure shows some more components of the N5316A test backplane board for PCIe 5 Gb/s.

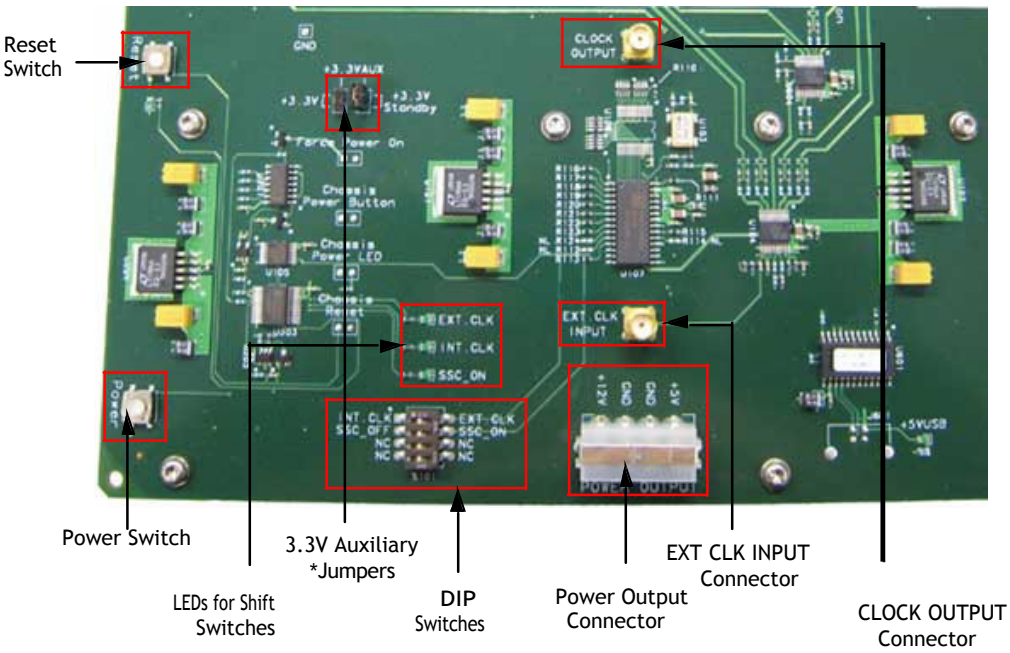


Figure 20 N5316A Backplane Board Components

As shown in the previous figure, the N5316A backplane board has:

- A *power switch*, which is used to switch off and on the power supply to the circuits of the board.

  This power switch is given in addition to the main power switch of the board. Therefore, switching ON the main power switch is a *prerequesite* to start using the backplane board.
- A *reset switch*, which resets all the circuits of the board.
- Four *DIP switches*:
  - One to choose between internal and external clock (*INT CLK* and *EXT CLK*).

  - One to choose between disabling and enabling SSC (*SSC_OFF* and *SSC_ON*).
  - The other two switches are not connected to the board.
- The following LEDs to show the status of above mentioned switches:
  - **EXT CLK**— It glows when the external clock is enabled.
  - **INT CLK**— It glows when the internal clock is enabled.
  - **SSC_ON**— It glows when you shift the above mentioned switch towards the SSC_ON label.
- A *CLOCK OUTPUT* connector, which provides a clock feed to an external device. You generally use this component when you want to synchronize an external device with the clock cycle of the backplane board.

  The specifications of CLOCK OUTPUT connector are:
  - *Terminate into 50 Ohm*
  - *Level — Approximately 800 mVpp*
- A *EXT CLK INPUT* connector, which is used to receive a clock feed for the backplane board from an external device. You generally use this component when you want to synchronize the backplane board with the clock cycle of an external device.

  The specifications of EXT CLK INTPUT connector are:
  - *AC coupled*
  - *Level — Approximately 800 mVpp*
- A *power output* connector, which has four pins: one +5V, one +12V, and two GND. Use these pins judicially to power-up an external module.
- Two *3.3V auxiliary jumpers*:
  - 3.3V is directly connected to the power switch, which means it turns on when you press the power switch.
  - 3.3V Standby is powered on as soon as the board is powered on by the main switch.

WARNING **Do not directly touch any component on the N5316A backplane board. It may be hot.**

AVERTISSEMENT **Ne touchez aucun composant du fond de panier N5316A. Il peut être chaud.**

CAUTION Components on the N5316A backplane board are sensitive to the static electricity. Therefore, take necessary anti-static precautions, such as wear a grounded wrist strap, to minimize the possibility of electrostatic damage.

CAUTION

During normal operations, N5316A operates safely. Nevertheless, the circuits of 3.3 V and 12 V on PCI Express connectors and 5 V on the Power Output connector are not limited and may provide currents higher than 8 A. In case of failure, for example short circuit, such a circuit presents the risk of causing fire. Therefore, to limit the energy and avoid damage, we urgently recommend implementing one of the following preventive measures:

1. Limit the circuits of your product under test with a 4A IEC fuse (5A UL fuse) at the input.

2. Operate the N5316A in a fire enclosure.

Table of electrical specification is given below:

U⎓Output	Imax Output
+3.3V	28A
+5V	42A
+12V	22A

ATTENTION

Le fond de panier fonctionne en toute sécurité dans des conditions normales. Les circuits de 3,3 et 12 V sur les connecteurs PCI Express et de 5 V sur le connecteur d'alimentation ne sont toutefois pas limités et peuvent fournir des courants de plus de 8 A. En cas de dysfonctionnement, comme un court-circuit, ce circuit présente un risque d'incendie. Pour limiter le courant et éviter des dommages, nous recommandons donc d'appliquer l'une des mesures préventives suivantes:

1. Limitez les circuits de votre produit testé avec un fusible IEC de 4 A (fusible UL de 5 A) à l'entrée.

2. Utilisez la carte N5316A dans un boîtier ignifuge.

Le tableau des spécifications électriques est fourni ci-dessous :

U de sortie, Imax de sortie

+3,3 V, 28 A

+5 V, 42 A

+12 V, 22 A

CAUTION Secondary circuits potentially provide currents higher than 8A.

Before connecting your device under test please carefully read the safety information and precautions in the installation guide.

ATTENTION Des courants de plus de 8 A peuvent circuler dans les circuits secondaires.

Avant de brancher votre appareil en test, veuillez lire attentivement les consignes et les précautions de sécurité figurant dans le manuel d'installation.

7 Soft Touch Midbus Probes

Midbus 2.0 (Full Size) Probes 40
N5328A Half Size Midbus Probe 62
Electrical Design Considerations for Midbus Probes 69
Reference Clock Probe 72

Agilent provides midbus 2.0 (full size) probes and the N5328A half size midbus probe. The half size midbus probe can be used in situations where space constraints in a board's design prevent having a full sized probe.

Both full size and half size midbus probes connect to soft touch footprints which must be designed into the device under test (DUT).

There are electrical design considerations that apply to both the full size and half size midbus probes.

Also, both full size and half size midbus probes provide a reference clock probe for situations where it is necessary to probe the reference clock from the DUT.

Midbus 2.0 (Full Size) Probes

This section introduces you to the Agilent midbus 2.0 probes. It also provides information on configuration support.

- "Overview and Configuration Support" on page 41
- "Installation Instructions" on page 41
- "Characteristics" on page 42
- "Mechanical Design Considerations for Midbus 2.0 Probes" on page 43
- "Electrical Design Considerations for the Midbus 2.0 Probes" on page 50

The Agilent midbus 2.0 series of probes using soft touch technology are specially designed to provide support for up to 16 channel probing solutions.

To integrate a midbus probe, a midbus probe footprint must be designed into the target board. A 3 pin header must also be designed into the target board if it is required to supply a reference clock to the protocol analyzer. This document is intended to provide information needed by platform and system design teams for integration of midbus 2.0 into their designs. It provides a mechanical and electrical solution space for Midbus Probe placement with the PCI Express bus.

Although information on PCI Express topology and specifications will be given, this document is not intended to take the place of other PCI Express design documentation. It is assumed that a design team utilizing this document for their design constraints will validate their designs through pre and post route electrical simulation and keep-out volume analysis.

Nomenclature

- N4241A refers to midbus 2.0 straight bi-directional x8 for PCIe 5 Gb/s.
- N4242A refers to midbus 2.0 swizzled x16 for PCIe 5 Gb/s.
- N4243A refers to midbus 2.0 split x4 for PCIe 5 Gb/s.
- Midbus connection, midbus probe, and midbus footprint refer to the Agilent midbus 2.0 footprint connector (N4241A/ N4242A/ N4243A) PCI Express compression cable set.
- "channel" refers to either an upstream differential pair OR downstream differential pair for a given lane. In other words, a "channel" refers to either a transmit-differential pair OR a receive-differential pair for a given lane.

Retention Modules

One kit of 5 retention modules is supplied with each N4241A, N4242A, and N4243A probes.

Contact your local sales representative to order additional retention modules:

- Part Number: E2960B-RET-05

RETENTION MODULES FOR MIDBUS PROBE 2.0 - 5 PCS.

- Part Number: E2960B-RET-50

  RETENTION MODULES FOR MIDBUS PROBE 2.0 - 50 PCS.

Overview and Configuration Support

Figure 21 Midbus Probe 2.0

Link Configuration Support

The midbus 2.0 offers a number of different probing options for different applications. The platform designer has the flexibility to configure a probing solution that best meets the needs of the system. With midbus 2.0 offering upto 16 channel probing solutions, the following configurations may be made*:

- Upstream and downstream channels of one x8 link.
- Upstream or downstream channels of one x16 link.
- Upstream or downstream channels of up to four x4, x2, or x1 links.

*As long as the Midbus Probe placement within the system requirements are met. System designers should verify that their system requirements are supported by the midbus 2.0 by contacting Agilent Technologies directly.

NOTE

Other combinations may be available. Contact Agilent Technologies for the latest support configurations.

Installation Instructions

- First solder and secure the retention module onto the device under test (DUT) on two sides of the midbus probe footprint.

- Select the midbus cable (straight, swizzle or split) that best suits the design. Connect the wide connector of midbus to the Protocol Analyzer module and tighten the thumbscrews.
- Identify the white bullet on the probe label indicating pin 1 as seen in Figure 1. Align it to the pin 1 on the layout board. (While designing the layout make sure pin 1 is defined and marked.) A vertically aligned probe is shown in the Figure 2.
- Slide the probe into the retention module and gently tighten the thumbscrews located at the top of the midbus probe head. A screwdriver may be used to ensure that there is a secure connection. The thumbscrews should be tightened to a snug fit but do not over tighten.

Figure 22 Midbus aligned over back plane

- Finally, if an external reference clock is to be supplied to protocol analyzer, connect the external clock cable (of the midbus) to the reference clock header on the target board.

Characteristics

CAUTION Other combinations may be available. Contact Agilent Technologies for the latest support configurations.

Probe Inputs:	Input Voltage: 25 V max or 3 V rms into 250 Ohms.
Temperature:	Operating 0 to 40 Deg C with 200 linear feet per minute airflow. Storage -40 to 70 Deg C.
Humidity:	Operating 15% to 95% non condensing.
Altitude:	Operating: to 3000 meters (10000 ft).
Airflow:	For a single probe with no heat sources within 1 inch, 140 linear feet per minute of air flow is required. For two probes, placed side by side with minimum spacing and no other heat sources within 1 inch, 200 linear feet per minute of air flow is required.

Mechanical Design Considerations for Midbus 2.0 Probes

This section contains information on mechanical design of the Midbus Probe and the reference clock pin header. It also provides details on footprint dimensions, keep- out volumes, and part numbers.

- "Footprint Dimensions and Specifications" on page 43
- "Connecting the Retention Module" on page 45
- "N5311 Midbus Interposer Card" on page 48

Footprint Dimensions and Specifications

Please ensure the following pre- requisites are met for the design:

- Solder mask must not extend above the pad height for a distance of .005 inches from the pad.
- Via-in-pad is allowed if the vias are filled level with the pad or the via hole size is less that .005 inches.
- Permissible surface finishes on pads are HASL, immersion silver, or gold over nickel. The height of the pads contacted by the probe must be within +/- .007 inches of the bottom surface of the retention module.

The Midbus probe 2.0 footprint, that needs to be designed into the target board can be observed in the following figure. The following figure displays the detailed layout dimensions for the footprint. Notice that the connector has 50 pins.

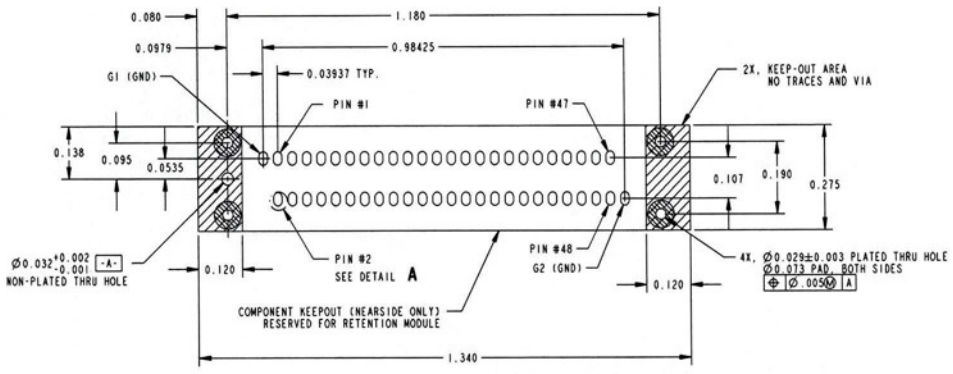


Figure 23 Midbus 2.0 footprint dimensions, pin numbering, and specification

The following figure displays detailed view of a pad with geometrical information on it.

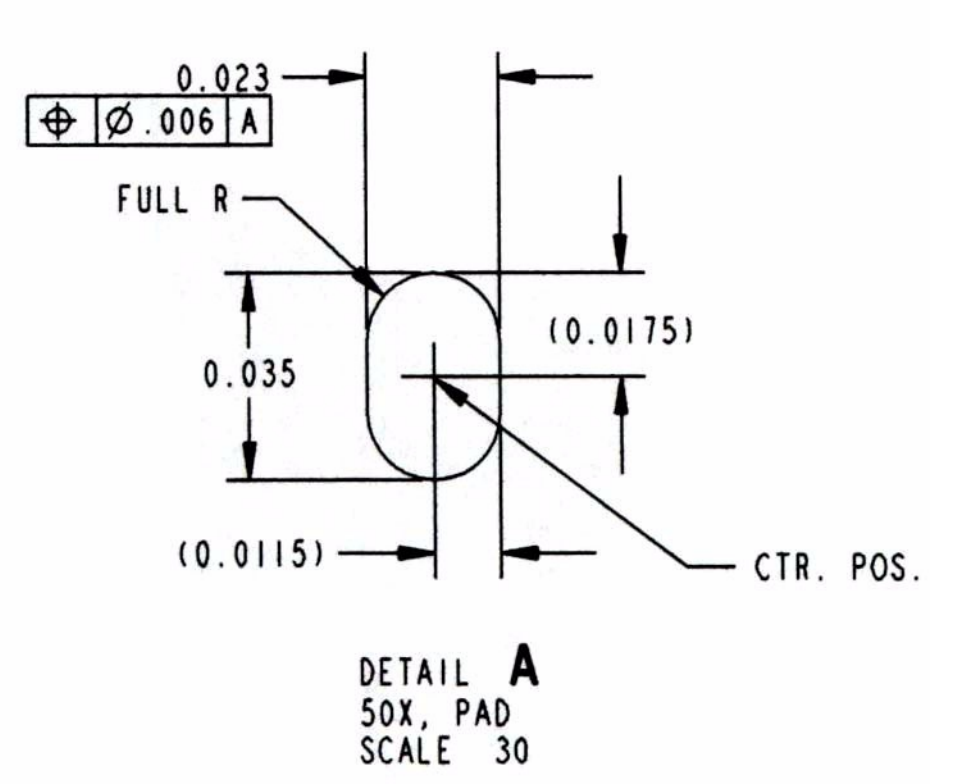


Figure 24 Detail A - detailed view of a pad.

Connecting the Retention Module

The retention module helps to connect midbus probe to the device under test (DUT). To achieve this, the retention module must be soldered onto the DUT. After this is done, the probe can be easily plugged into this retention module.

The following figure displays the dimensions of the midbus probe, which is plugged into the retention module.

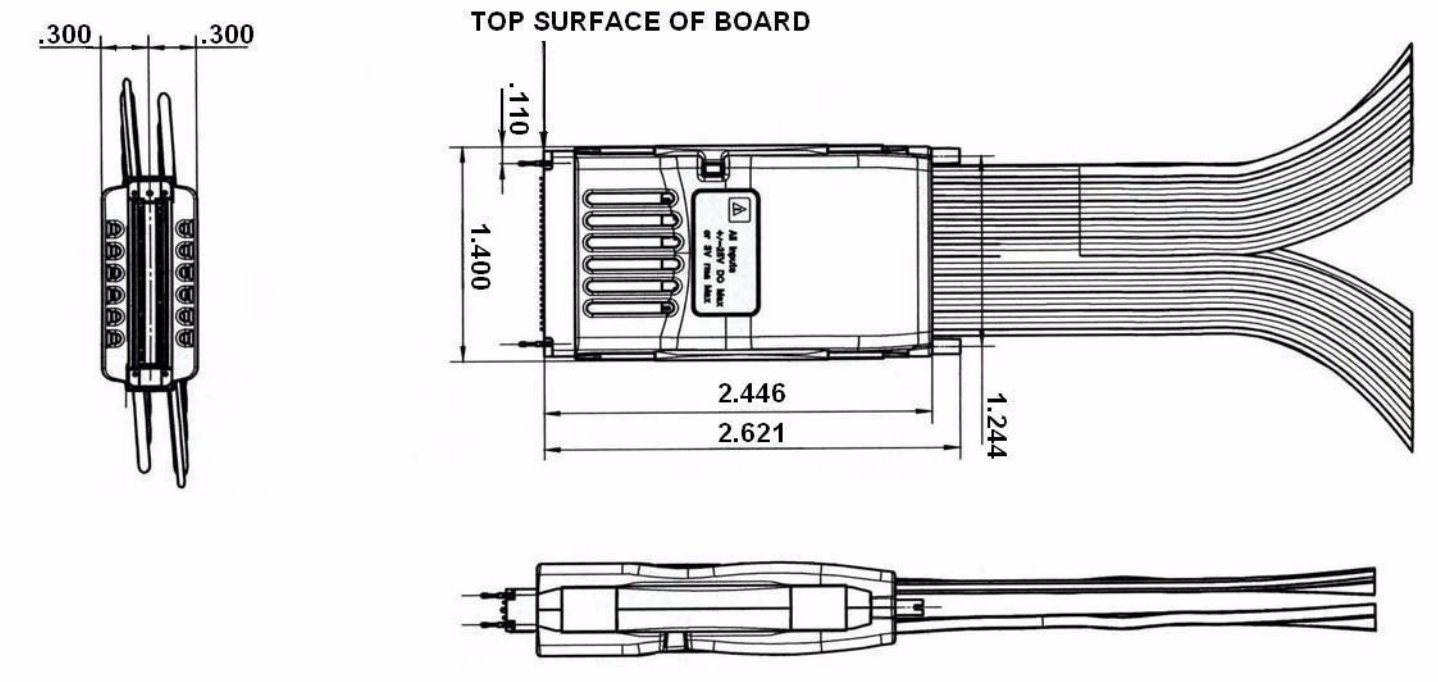


Figure 25 Midbus probe plugged into the retention module

The following figure displays the retention module.

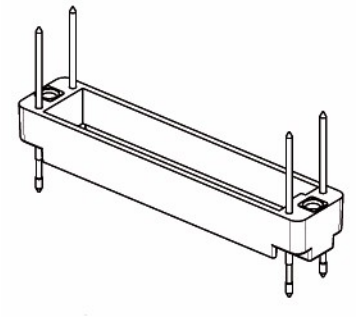


Figure 26 Retention module

The following figures show the dimensions of the retention module from different views.

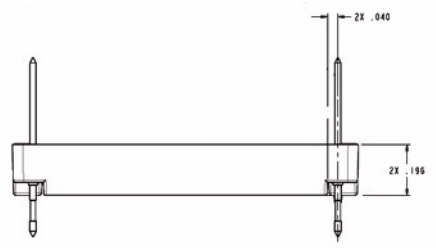


Figure 27 Dimensions of the Retention Module and its Parts

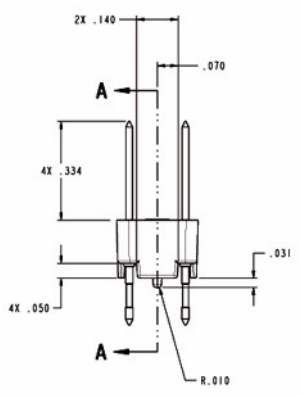


Figure 28 Dimensions of the Retention Module and its Parts

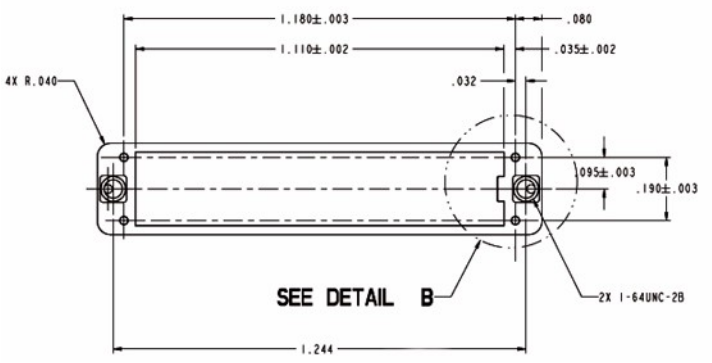


Figure 29 Dimensions of the Retention Module and its Parts

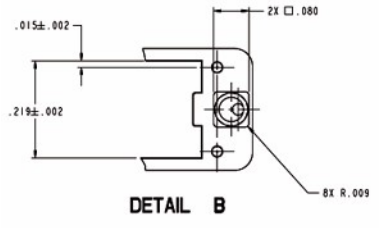


Figure 30 Dimensions of the Retention Module and its Parts

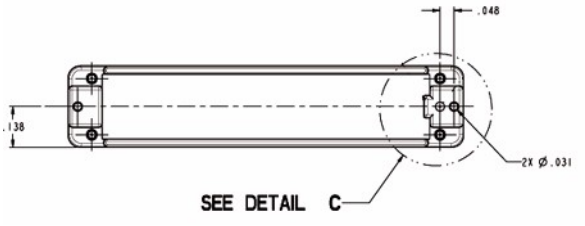


Figure 31 Dimensions of the Retention Module and its Parts

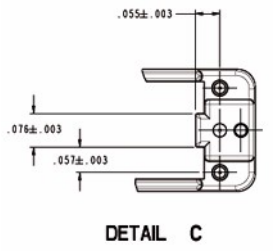


Figure 32 Dimensions of the Retention Module and its Parts

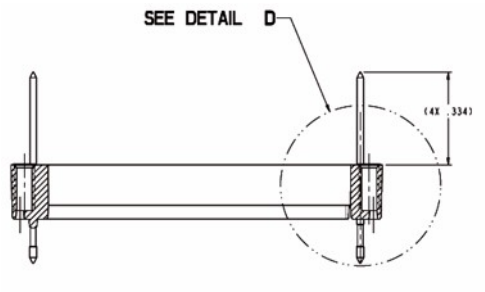


Figure 33 Dimensions of the Retention Module and its Parts

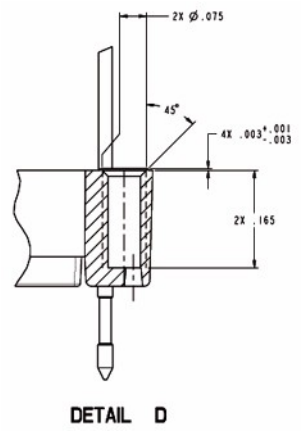


Figure 34 Dimensions of the Retention Module and its Parts

N5311 Midbus Interposer Card

The N5311 Midbus Interposer card provides the ability to capture the traffic between the two components when footprints are not available.

The following figure displays the dimensions of N5311 in millimeters (mm). The lower connector varies depending on the link width (x1, x4, x8, or x16). Also, the retention module on the right is only available for x16.

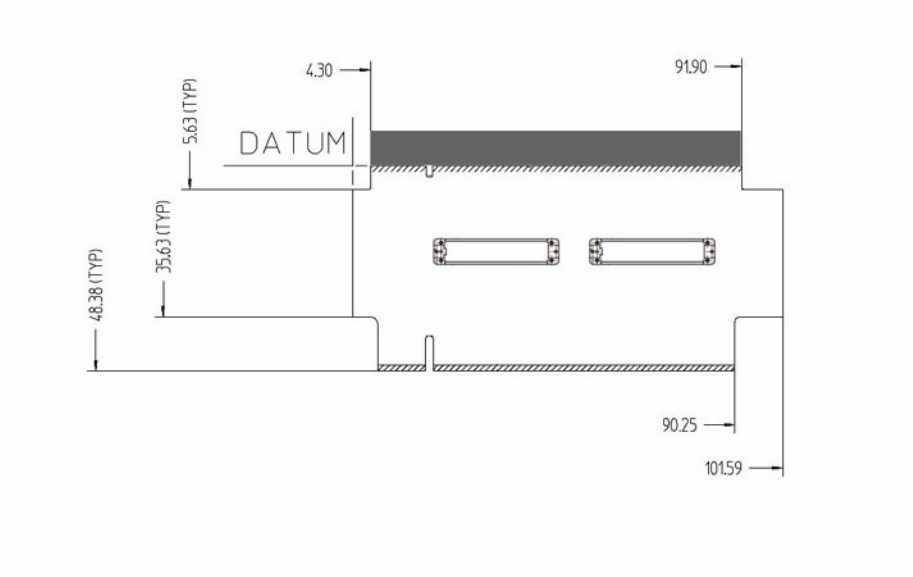


Figure 35 N5311 Midbus Interposer

Depending on the type of midbus probe, the N5311 Midbus Interposer card is available in the following flavors:

- For N4241A Midbus Probe:
  - N5311-66401 (x1 Midbus Interposer)
  - N5311-66404 (x4 Midbus Interposer)
  - N5311-66408 (x8 Midbus Interposer)
  - N5311-66426 (x16 Midbus Interposer). With this flavor of midbus interposer, maximum two N4241A midbus probes can be connected. This midbus interposer card routes one direction on each retention module.

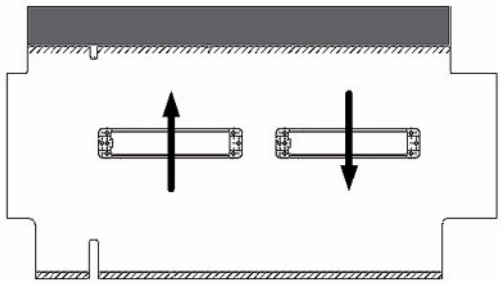


Figure 36 N5311-66426 Midbus Interposer Card

- For N4242A Midbus Probe:
  - N5311-66416 (x16 Midbus Interposer). With this flavor of midbus interposer, only one N4242A Probes can be connected. This midbus interposer card routes lane 0 … 7, bi-directional to the retention module on the left and lane 8…15, bi-directional to the retention module on the right (Figure 10).

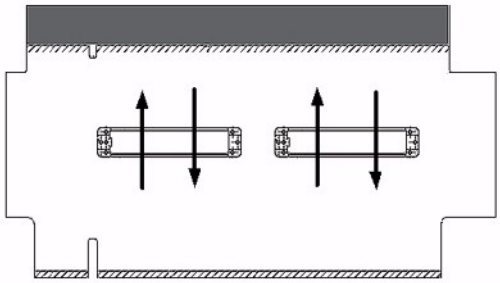


Figure 37 N5311-66416 Midbus Interposer Card

Electrical Design Considerations for the Midbus 2.0 Probes

This section contains specific electrical design details of the midbus 2.0 (full size) probes. These specific details include midbus routing suggestions and pin assignments.

These specific electrical design details are in addition to the general electrical design details that apply to all midbus probes (including the N5328A half size midbus probe). The general electrical design details include analyzer eye requirement definition, system impact due to midbus probe presence, and load models. See "Electrical Design Considerations for Midbus Probes" on page 69.

Also, see the electrical design details for the reference clock probe (which is the same for full size and half size midbus probes. See "Reference Clock Probe" on page 72.

The PCI Express Gen2 analyzer offers different probing options for different applications to suit different footprints on the device under test (DUT).

- "Routing considerations near/through PCI Express midbus footprint" on page 51
- "PCI Express Midbus Pin Assignments Overview" on page 52
- "General Probing Option and Pin Assignments" on page 53
- "Straight Probing Option and Pin Assignments" on page 54

- "Swizzled x16 Probing Option and Pin Assignments" on page 57
- "Split x4 Probing Option and Pin Assignments" on page 60

Routing considerations near/through PCI Express midbus footprint

Agilent will provide detailed information on routing and design considerations at a later date. The following figures present suggested routing for footprint negotiation in the case of surface (microstrip) routing when this routing is on the same side of the board as midbus.

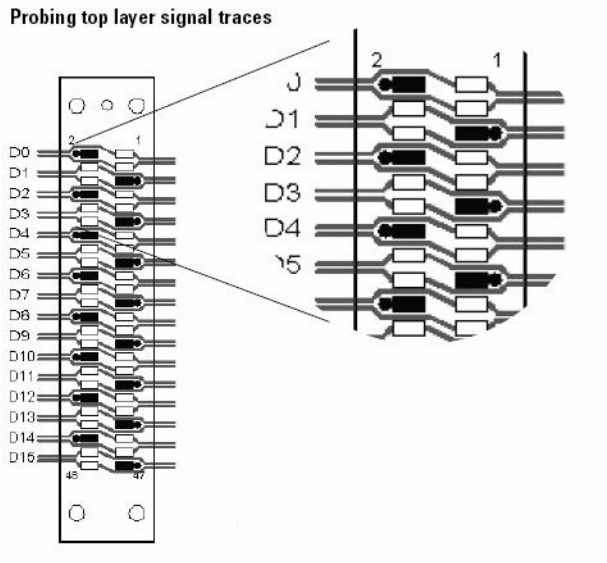


Figure 38 Suggested routing for microstrip traces on same layer as midbus

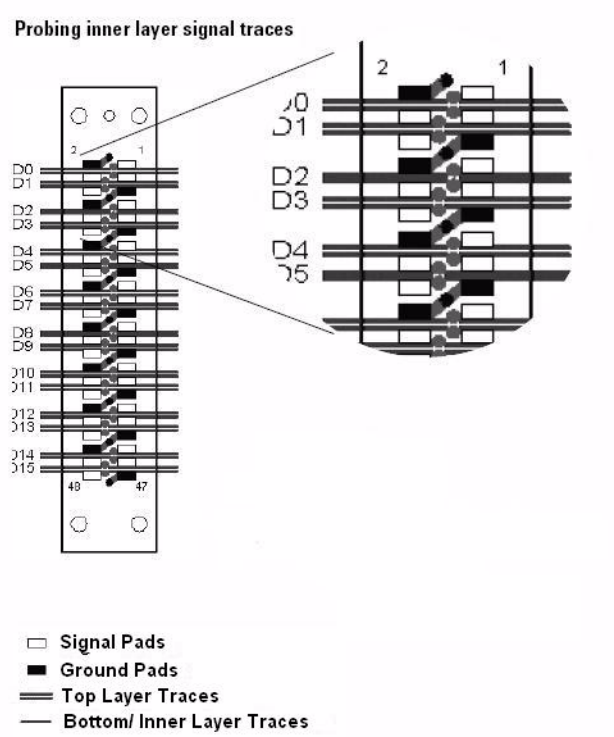


Figure 39 Inner layer and secondary side routing (surface layer opposite of midbus)

PCI Express Midbus Pin Assignments Overview

There is flexibility in the arrangement and layout of the midbus footprint. Agilent will provide configuration of the midbus to support the following midbus layouts. There is a detailed view of these connections below.

The pinout for the PCI Express midbus is given in "General Probing Option and Pin Assignments" on page 53. It is imperative that designers understand there is some freedom associated with the pin/signal assignment relationship. These notes are given here:

Footprint channel vs. lane/link designations	• Channel = either an upstream OR downstream differential pair for a given lane • C<letter> = the designator for a Channel which accepts a given differential pair of signals • C<letter><p or n> = the two signals of the differential pair. The signals within a given pair may be assigned to either p or n regardless of polarity
General rules for signal pair assignment	The differential pairs that make up the PCI Express links must be assigned to specific pins of the footprint. However, there is some freedom in this pair assignment in order to minimize routing constraints on the platform. Additionally, note that the channel to footprint assignment configuration is closely related to the "direction" of the probed link. More specifically, a bi-directional pin assignment is different from a unidirectional pin assignment. See the following tables contained in this section for more information.

General Probing Option and Pin Assignments

Table 1 General PCI Express midbus pinout

Pin #	Signal Name	Pin #	Signal Name
		G1	GND
2	GND	1	CAp
4	CBp	3	CAn
6	CBn	5	GND
8	GND	7	CCp
10	CDp	9	CCn
12	CDn	11	GND
14	GND	13	CEp
16	CFp	15	CEn
18	CFn	17	GND
20	GND	19	CGp
22	CHp	21	CGn
24	CHn	23	GND
26	GND	25	CIp
28	CJp	27	CIn
30	CJn	29	GND
32	GND	31	CKp

Table 1 General PCI Express midbus pinout (continued)

Pin #	Signal Name	Pin #	Signal Name
34	CLp	33	CKn
36	CLn	35	GND
38	GND	37	CMp
40	CNp	39	CMn
42	CNn	41	GND
44	GND	43	CPp
46	CQp	45	CPn
48	CQn	47	GND
G2	GND		

Straight Probing Option and Pin Assignments

This type of probe connects all 16 differential pairs of one probe head to one I/O module. In case of a uni-directional pin configuration it can be used to probe a single direction of a x1...x16 link (see Table 4), and in case of bi-directional configuration it can be used to probe both directions of a x1...x8 link (see Table 5).

NOTE

The midbus probe cable comes with two wires: brown and yellow. Out of these wires, only brown cable is supported for applying external clock.

Table 2 x16 (standard) PCI Express midbus pinout[1, 2, 3, 4]

Pin #	Signal Name	Pin #	Signal Name
		G1	GND
2	GND	1	C0p
4	C1p	3	C0n
6	C1n	5	GND
8	GND	7	C2p
10	C3p	9	C2n
12	C3n	11	GND
14	GND	13	C4p
16	C5p	15	C4n
18	C5n	17	GND

Table 2 x16 (standard) PCI Express midbus pinout[1, 2, 3, 4] (continued)

Pin #	Signal Name	Pin #	Signal Name
20	GND	19	C6p
22	C7p	21	C6n
24	C7n	23	GND
26	GND	25	C8p
28	C9p	27	C8n
30	C9n	29	GND
32	GND	31	C10p
34	C11p	33	C10n
36	C11n	35	GND
38	GND	37	C12p
40	C13p	39	C12n
42	C13n	41	GND
44	GND	43	C14p
46	C15p	45	C14n
48	C15n	47	GND
G2	GND		

[1] Polarity (p and n) of each differential pair may be swapped.
[2] This configuration can only probe either upstream 16 channels OR 16 downstream channels with one midbus. Please see Table 5 for a configuration that supports interleaved x16 traffic amongst two midbus footprints.
[3] Entire link assignment may be reversed in midbus. For example, channel 0 may be swapped in above table with channel 15, channel 1 with channel 14, etc. If swapping upstream, must also swap downstream (and vice versa).
[4] Analyzer supports probing of one link with smaller link width (x1, x2, x4, x8) on natural lane boundaries, e.g. a x4 link can be probed on lanes 0...3, 4...7, 8...11 or 12...15.

Table 3 x8 (straight, bi-directional) specific PCI Express midbus pinout[1, 2, 3, 4, 5]

Pin #	Signal Name	Pin #	Signal Name
		G1	GND
2	GND	1	C0p- Upstream
4	C0p- Downstream	3	C0n- Upstream
6	C0n- Downstream	5	GND
8	GND	7	C1p- Upstream

Table 3 x8 (straight, bi-directional) specific PCI Express midbus pinout[1, 2, 3, 4, 5]

Pin #	Signal Name	Pin #	Signal Name
10	C1p- Downstream	9	C1n- Upstream
12	C1n- Downstream	11	GND
14	GND	13	C2p- Upstream
16	C2p- Downstream	15	C2n- Upstream
18	C2n- Downstream	17	GND
20	GND	19	C3p- Upstream
22	C3p- Downstream	21	C3n- Upstream
24	C3n- Downstream	23	GND
26	GND	25	C4p- Upstream
28	C4p- Downstream	27	C4n- Upstream
30	C4n- Downstream	29	GND
32	GND	31	C5p- Upstream
34	C5p- Downstream	33	C5n- Upstream
36	C5n- Downstream	35	GND
38	GND	37	C6p- Upstream
40	C6p- Downstream	39	C6n- Upstream
42	C6n- Downstream	41	GND
44	GND	43	C7p- Upstream
46	C7p- Downstream	45	C7n- Upstream
48	C7n- Downstream	47	GND
G2	GND		

[1] Polarity (p and n) of each differential pair may be swapped.

[2] Can probe upstream 8 channels AND downstream 8 channels with one midbus.

[3] Entire link assignment may be reversed in midbus. For example, channel 0-upstream may be swapped in above table with channel 7-upstream, channel 1-upstream with channel 6-upstream, etc. If swapping upstream, must also swap downstream (and vice versa).

[4] Upstream and downstream pin assignments may be swapped. For example, channel 0-upstream may be swapped with channel 0-downstream, etc. Note that if one channel of upstream swapped with downstream, all channels upstream and downstream channels must be swapped.

[5] Analyzer supports probing of one bi-directional link with smaller link width (x1, x2, x4) on natural lane boundaries, e.g. a x4 link can be probed on lanes 0...3 or 4...7

Swizzled x16 Probing Option and Pin Assignments

This type of probe is used in cases where a x16 link is split up onto two footprints in such a way that lanes 0...7 of both directions are on one footprint and lanes 8...15 of both directions are on the other. The swizzled probe connects two probe heads to two I/O modules in a way that each of the I/O modules receives all 16 channels of one direction.

The following figure displays a N4242A swizzled x16 midbus probe cable.

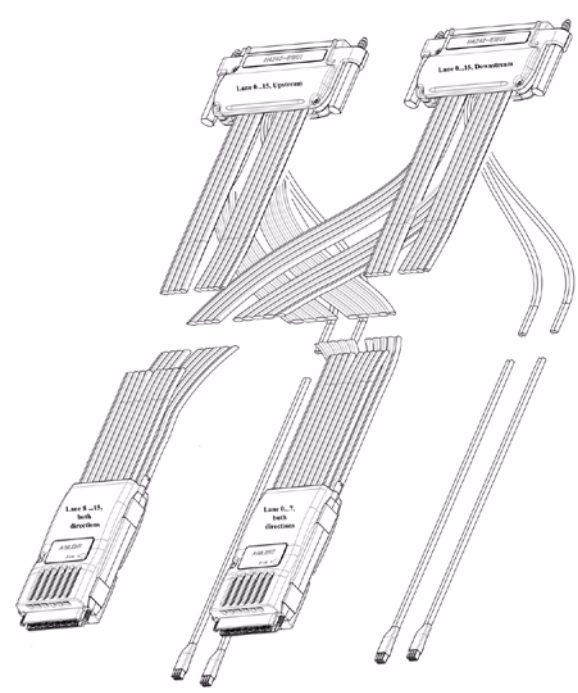


Figure 40 N4242A Swizzled x16 Midbus Probe

NOTE

The midbus probe cable comes with two wires: brown and yellow. Out of these wires, only brown cable is supported for applying external clock.

The probe heads are labeled Lane 0 ...7, both directions and Lane 8 ...15, both directions. The Lane 0 ...7, both directions probe head must be plugged into the footprint that carries lanes 0...7, whereas the Lane 8 ...15, both directions probe head must be plugged into the footprint that carries lanes 8...15 (Table 6).

Table 4 Swizzled x16 PCI Express midbus pinout[1, 2, 3, 4, 5]

Midbus Footprint for lanes 0...7				Midbus footprint for lanes 8...15			
Pin #	**Signal Name**	**Pin #**	**Signal Name**	**Pin #**	**Signal Name**	**Pin #**	**Signal Name**
		G1	GND			G1	GND
2	GND	1	C0p- Upstream	2	GND	1	C8p- Upstream
4	C0p- Downstream	3	C0n- Upstream	4	C8p- Downstream	3	C8n- Upstream
6	C0n- Downstream	5	GND	6	C8n- Downstream	5	GND
8	GND	7	C1p- Upstream	8	GND	7	C9p- Upstream
10	C1p- Downstream	9	C1n- Upstream	10	C9p- Downstream	9	C9n- Upstream
12	C1n- Downstream	11	GND	12	C9n- Downstream	11	GND
14	GND	13	C2p- Upstream	14	GND	13	C10p- Upstream
16	C2p- Downstream	15	C2n- Upstream	16	C10p- Downstream	15	C10n- Upstream
18	C2n- Downstream	17	GND	18	C10n- Downstream	17	GND
20	GND	19	C3p- Upstream	20	GND	19	C11p- Upstream
22	C3p- Downstream	21	C3n- Upstream	22	C11p- Downstream	21	C11n- Upstream
24	C3n- Downstream	23	GND	24	C11n- Downstream	23	GND
26	GND	25	C4p- Upstream	26	GND	25	C12p- Upstream
28	C4p- Downstream	27	C4n- Upstream	28	C12p- Downstream	27	C12n- Upstream
30	C4n- Downstream	29	GND	30	C12n- Downstream	29	GND
32	GND	31	C5p- Upstream	32	GND	31	C13p- Upstream
34	C5p- Downstream	33	C5n- Upstream	34	C13p- Downstream	33	C13n- Upstream
36	C5n- Downstream	35	GND	36	C13n- Downstream	35	GND
38	GND	37	C6p- Upstream	38	GND	37	C14p- Upstream
40	C6p- Downstream	39	C6n- Upstream	40	C14p- Downstream	39	C14n- Upstream
42	C6n- Downstream	41	GND	42	C14n- Downstream	41	GND
44	GND	43	C7p- Upstream	44	GND	43	C15p- Upstream
46	C7p- Downstream	45	C7n- Upstream	46	C15p- Downstream	45	C15n- Upstream
48	C7n- Downstream	47	GND	48	C15n- Downstream	47	GND

Table4 Swizzled x16 PCI Express midbus pinout[1, 2, 3, 4, 5] (continued)

Midbus Footprint for lanes 0...7					Midbus footprint for lanes 8...15			
Pin #	**Signal Name**	**Pin #**	**Signal Name**		**Pin #**	**Signal Name**	**Pin #**	**Signal Name**
G2	GND				G2	GND		

[1] Polarity (p and n) of each differential pair may be swapped.

[2] Can probe upstream 16 channels and downstream 16 channels with swizzled x16 probe.

[3] Entire link assignment may be reversed in midbus. For example, channel 0-upstream may be swapped in above table with channel 7-upstream, channel 1-upstream with channel 6-upstream, etc. If swapping upstream, must also swap downstream (and vice versa) and if swapping footprint A, must also swap footprint B.

[4] Upstream and downstream pin assignments may be swapped. For example, channel 0-upstream may be swapped with channel 0-downstream, etc. Note that if one channel of upstream swapped with downstream, all channels upstream and downstream channels must be swapped.

[5] Analyzer supports probing of one bi-directional link with smaller link width (x1, x2, x4, x8) on natural lane boundaries, e.g. a x4 link can be probed on lanes 0...3, 4...7, 8...11 or 12...15.

To use the N4242A swizzled x16 midbus probe

1. Plug the probe head labeled Lane 0 ...7, both directions into the retention module carrying lane 0 to 7.

   In the following figure, that is the retention module on the right.

2. Plug the probe head labeled Lane 8 ...15, both directions into the retention module carrying lane 8 to 15.

   In the following figure, that is the retention module on the left. Older probes might be labeled B.

NOTE Older probes might be labeled A instead of Lane 0 ...7, both directions and B instead of Lane 8 ...15, both directions. In case you are using a probe marked B, then this probe must be plugged in 180 degrees rotated.

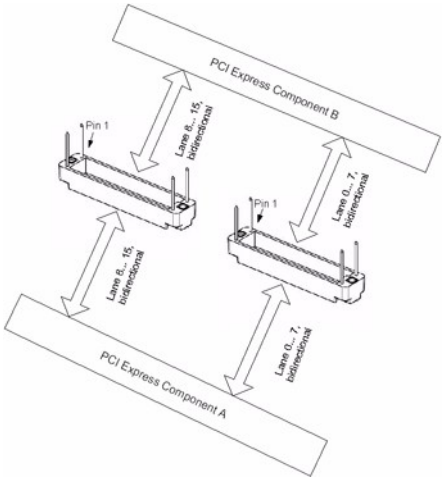


Figure 41 Connecting Swizzled x16 to Retention and I/O Modules

3 Plug the module connector labeled Lane 0 …15, upstream into an N5306A I/O module.

4 Plug the module connector labeled Lane 0 …15, downstream into a different N5306A I/O module.

5 In the Protocol Analyzer GUIs for both of the N5306A I/O modules, select the probe type for swizzled probes in the Hardware Setup dialog box.

Remember that one module is now capturing upstream traffic only while the other is capturing downstream traffic only. In order to view both directions in one listing, add both analyzers to a single session.

Split x4 Probing Option and Pin Assignments

This type of probe is used to probe two bi-directional x1…x4 links on the same footprint simultaneously. The split x4 probe connects one probe head to two I/O modules in such a way that each I/O module analyzes one of the bi-directional links (see Table 8).

Table 5 Dual x4 (bi-directional)

Pin #	Signal Name	Pin #	Signal Name
		G1	GND
2	GND	1	C0p- Upstream1
4	C0p- Downstream1	3	C0n- Upstream1
6	C0n- Downstream1	5	GND
8	GND	7	C1p- Upstream1

Table 5 Dual x4 (bi-directional) (continued)

Pin #	Signal Name	Pin #	Signal Name
10	C1p- Downstream1	9	C1n- Upstream1
12	C1n- Downstream1	11	GND
14	GND	13	C2p- Upstream1
16	C2p- Downstream1	15	C2n- Upstream1
18	C2n- Downstream1	17	GND
20	GND	19	C3p- Upstream1
22	C3p- Downstream1	21	C3n- Upstream1
24	C3n- Downstream1	23	GND
26	GND	25	C0p- Upstream2
28	C0p- Downstream2	27	C0n- Upstream2
30	C0n- Downstream2	29	GND
32	GND	31	C1p- Upstream2
34	C1p- Downstream2	33	C1n- Upstream2
36	C1n- Downstream2	35	GND
38	GND	37	C2p- Upstream2
40	C2p- Downstream2	39	C2n- Upstream2
42	C2n- Downstream2	41	GND
44	GND	43	C3p- Upstream2
46	C3p- Downstream2	45	C3n- Upstream2
48	C3n- Downstream2	47	GND
G2	GND		

N5328A Half Size Midbus Probe

- "Setting Up the Probe" on page 64
- "Footprint Pinout of the Probe" on page 64
- "Mechanical Dimensions" on page 65

This chapter provides information on the N5328A half size midbus probe used for PCIe.

There are situations when the space constraints in a board's design prevent having a full sized probe to capture and debug signals. In such situations, the customer compromises and creates a half sized foot print instead. For such situations, Agilent provides the N5328A half size midbus probe, which you can connect to the smaller foot prints to capture the traffic.

The N5328A half size midbus probe supports two different footprints: *straight* and *alternate*.

The following figure shows the N5328A half size midbus probe cable.

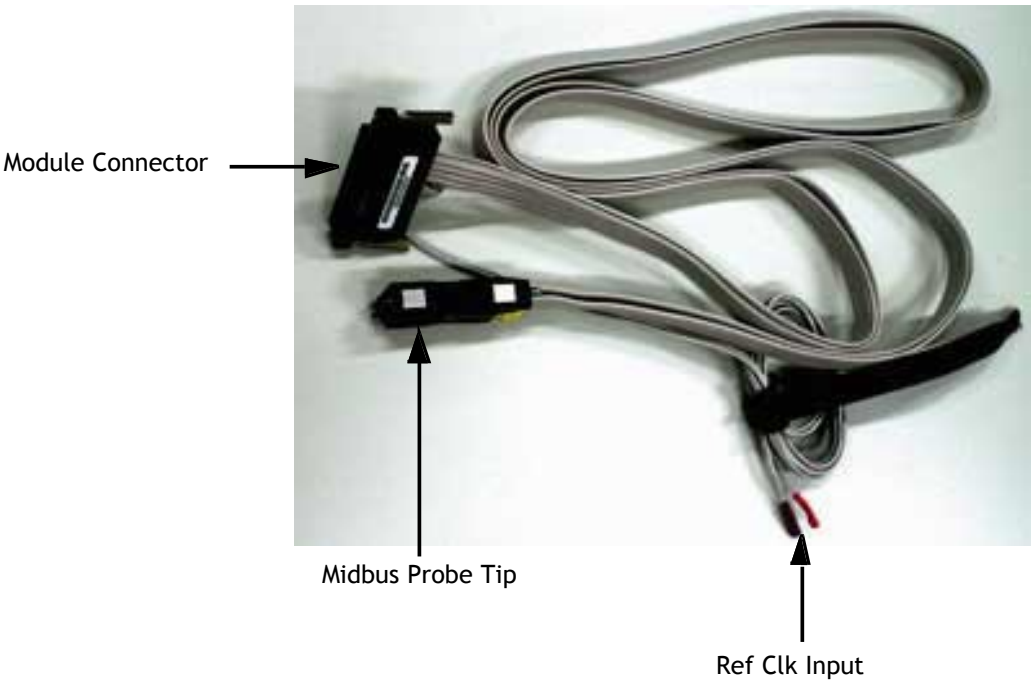


Figure 42 N5328A Half Size Midbus Probe

Components shown in the above figure are described below:

- **Module Connector**— This component connects to the *Analyzer Probe* component of the N5306A I/O module.

  For information on N5306A I/O module, see Chapter 1, “N5306A I/O Module,” starting on page 7.

- **Midbus Probe Tip**— This component connects to half size foot print on the board. The following figure shows the midbus probe tip plugged into the retention module for the half size foot print on the backplane board.

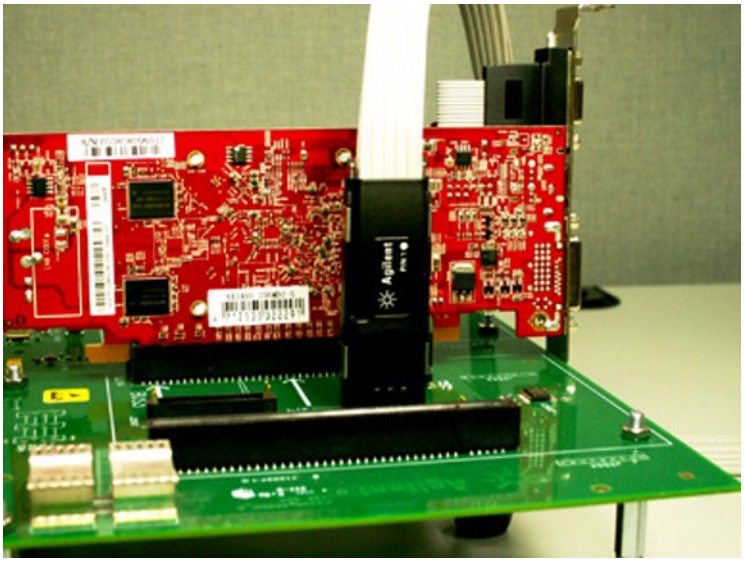


Figure 43 Connecting Midbus Probe Tip

NOTE For information on retention modules, see Chapter 6, “N5316A Backplane Board for PCIe,” starting on page 33.

WARNING **Do not directly touch any component on the N5328A half size midbus probe. It may be hot.**

CAUTION Components on the N5328A half size midbus probe are sensitive to the static electricity. Therefore, take necessary anti-static precautions, such as wear a grounded wrist strap, to minimize the possibility of electrostatic damage.

Setting Up the Probe

To setup the probe cable:

1 Solder and secure the retention module on DUT from two sides of the midbus probe footprint.

2 Connect **Module Connector** of the probe cable into the **Analyzer Probe** slot on the N5306A I/O module.

3 Plug the midbus probe Tip into the retention module on the backplane board.

To do this:

a Align the *PIN 1* label (adjacent to the *white bullet*) on the probe with the PIN 1 label on the layout board.

b Slide the midbus probe Tip into the retention module and gently tighten the thumbscrews located at the top of the midbus probe Tip. The thumbscrews should be tightened to a snug fit, but do not over tighten. If needed, you can use a screwdriver to ensure a secure connection.

4 Do the following if you need to supply an external reference clock to Protocol Analyzer:

- Connect the **Ref Clk Input** cables to the reference clock header of the target board.

Footprint Pinout of the Probe

The following table shows the pinout arrangement for the straight half size midbus probe footprint.

Table6 Footprint pinout for straight half size midbus probe

Pin #	Signal Name	Pin #	Signal Name
		G1	GND
2	GND	1	C0p - Upstream
4	C0p - Downstream	3	C0n - Upstream
6	C0n - Downstream	5	GND
8	GND	7	C1p - Upstream
10	C1p - Downstream	9	C1n - Upstream
12	C1n - Downstream	11	GND
14	GND	13	C2p - Upstream
16	C2p - Downstream	15	C2n - Upstream
18	C2n - Downstream	17	GND

Table6 Footprint pinout for straight half size midbus probe (continued)

Pin #	Signal Name	Pin #	Signal Name
20	GND	19	C3p - Upstream
22	C3p - Downstream	21	C3n - Upstream
24	C3n - Downstream	23	GND
G2	GND		

The following table shows the pinout arrangement for the alternate half size midbus problem footprint.

Table7 Footprint pinout for alternate half size midbus probe

Pin #	Signal Name	Pin #	Signal Name
		G1	GND
2	GND	1	C0p - Upstream
4	C1p - Upstream	3	C0n - Upstream
6	C1n - Upstream	5	GND
8	GND	7	C2p - Upstream
10	C3p - Upstream	9	C2n - Upstream
12	C3n - Upstream	11	GND
14	GND	13	C0p - Downstream
16	C1p - Downstream	15	C0n - Downstream
18	C1n - Downstream	17	GND
20	GND	19	C2p - Downstream
22	C3p - Downstream	21	C2n - Downstream
24	C3n - Downstream	23	GND
G2	GND		

Mechanical Dimensions

Please ensure the following prerequisites are met for the design:

- Solder mask must not extend above the pad height for a distance of .005 inches from the pad.
- Via- in- pad is allowed if the vias are filled level with the pad or the via hole size is less that .005 inches.

- Permissible surface finishes on pads are HASL, immersion silver, or gold over nickel. The height of the pads contacted by the probe must be within +/- .007 inches of the bottom surface of the retention module.

The half size midbus probe footprint that needs to be designed into the target board can be observed in the following figure. The figure displays the detailed layout dimensions for the footprint. Notice that the half size midbus probe softouch connector has 26 pins, but figure shows only 24 pins.

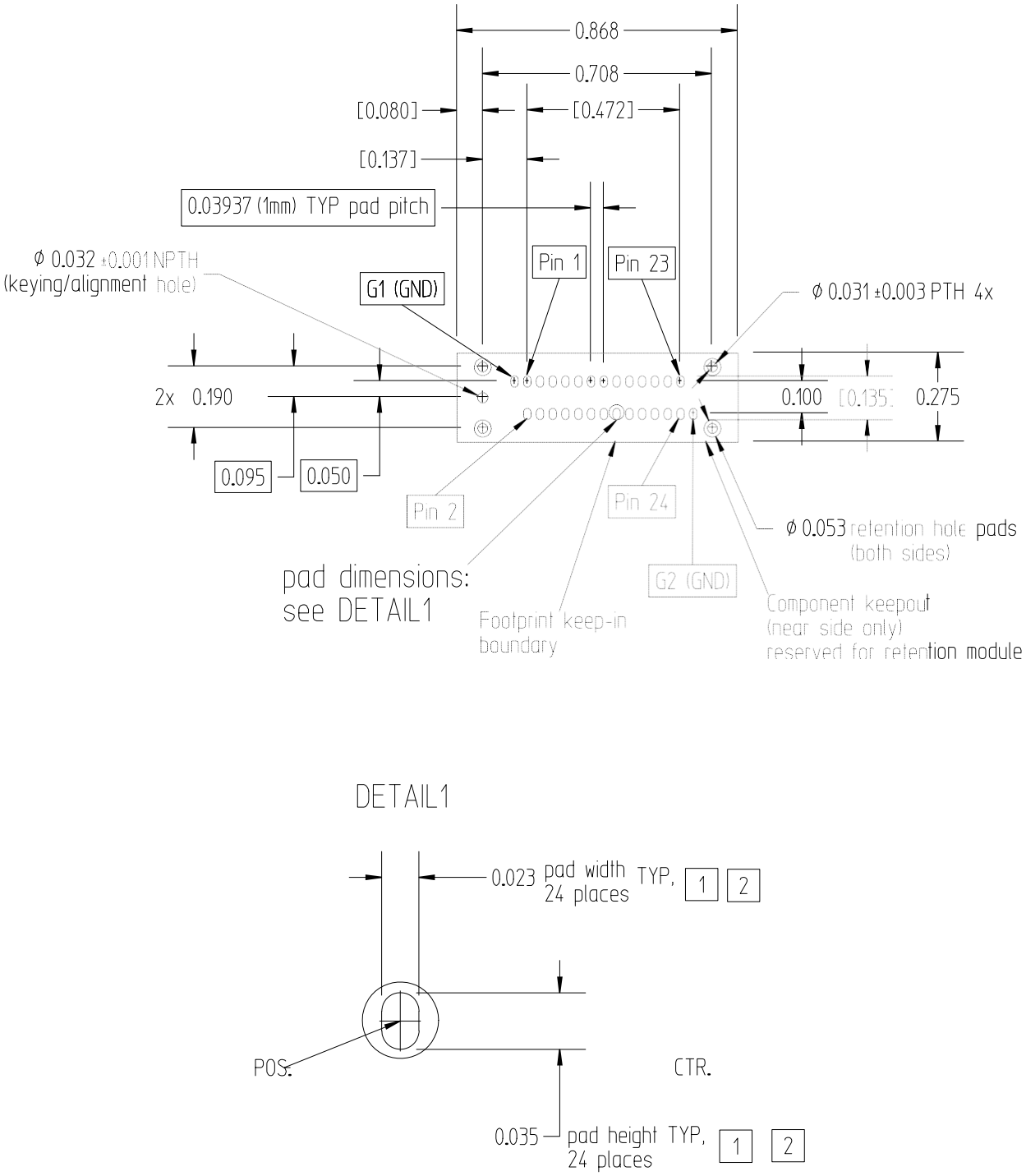


Figure 44 Dimensions of N5328A

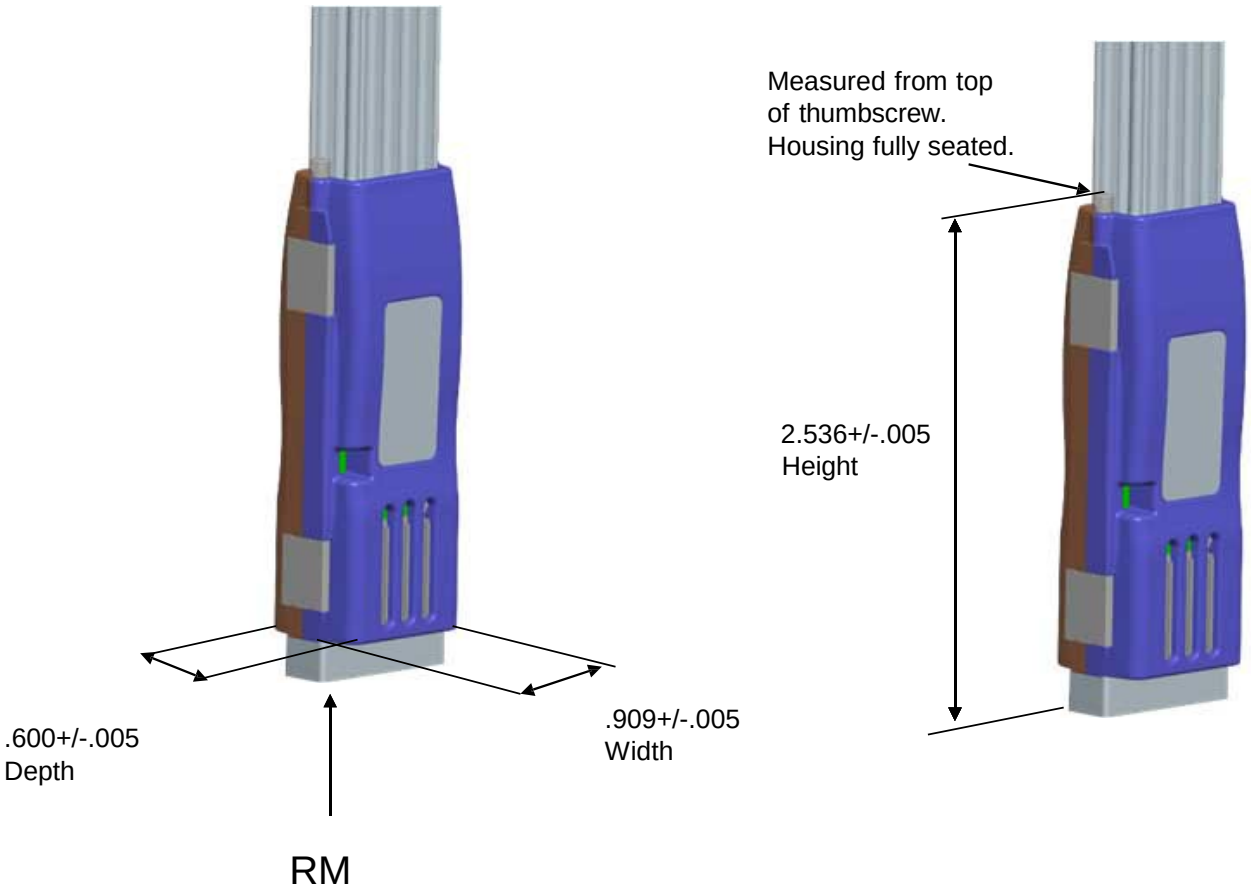


Figure 45 Half size midbus keepout volume

Electrical Design Considerations for Midbus Probes

This section contains electrical design details and reference clock pin header of the midbus 2.0 series of probes using soft touch technology. These details include analyzer eye requirement definition, system impact due to midbus probe presence, midbus routing suggestions, load models, and pin assignments.

Logical probing of the PCI Express bus is achieved through tapping a small amount of energy off the probed signals and channelling this energy to the logic analyzer. In order to avoid excessive loading conditions, the use of tip resistors, or isolation resistors, is employed. These relatively high impedance tip resistors enable the logic analyzer to sample bus traffic without significantly loading the probed signals. A high-level block diagram of a generic PCI Express bus with a logic analyzer interface is given in the following figure. Note that this would be repeated for each differential pair within a PCI Express link.

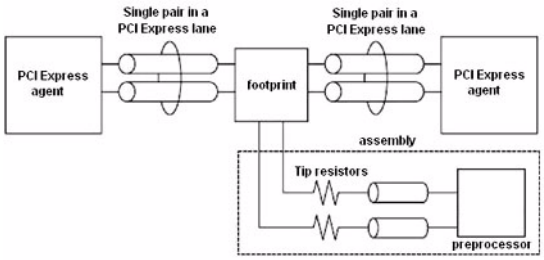


Figure 46 Block diagram example of a generic PCI Express bus with a protocol analyzer

Midbus Placement Within System Topology

For analyzer to reliably capture logical transactions on the bus, adequate signal eye must be made available to the midbus. It is incumbent upon the platform designers to ensure that sufficient signal eye is available to the midbus while the midbus load is in place so that proper signal capture can be performed. This must be verified via electrical simulation utilizing the load model provided in the Load model for midbus probe figure.

The eye requirements are measured by eye height and eye width, forming a diamond shape. These requirements are described pictorially in the following figure.

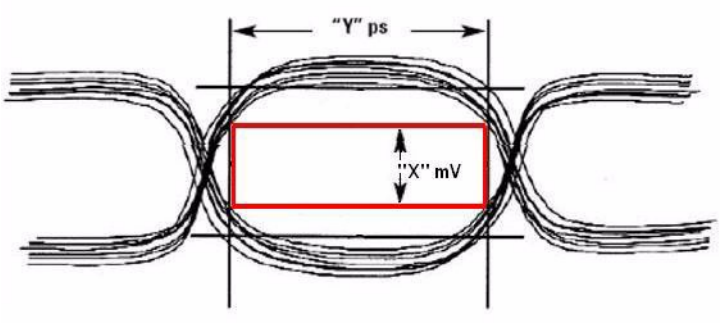


Figure 47 Example of eye specifications as seen at the midbus pad

The following table details the specific eye requirements for Agilent Technologies. Address questions to Agilent Technologies for the most current eye requirements.

Table 8 PCI Express midbus footprint placement interconnect specification

	Agilent Technologies Specification
Min. eye height at midbus pad[1]	60 mV
Min. eye width at midbus pad	0.6 UI (120 ps at midbus footprint), that is, Jitter tolerance of 0.4 UI
Length matching requirements of the P/N sides of the differential pairs[2]	±5 mil
Length matching requirements -pair to pair	same as PCI Express specification
[1] Measured in differential units, for example, Vppdiff = |2*(Vp – Vn)| [2] Interconnect must length match ±5 mils from source to midbus footprint pad for each polarity of the differential pair	

The eye characteristics given in the above table must be maintained for all probed channels, regardless of direction. Overall, these midbus placement specifications limit the electrical distance between the driver pin and the midbus attach point. Conceivably, probing both directions in lanes of a long PCI Express link may require two separate footprints and midbus assemblies, while probing both directions of relatively short links may be accomplished with one midbus. Regardless of implementation, refer to usage restrictions as listed in the "Overview and Configuration Support" section. The same midbus eye requirements exist for all links substrates (for example, FR4, cables, etc.).

An additional constraint on midbus footprint placement involves the relative location of the AC coupling capacitors. The capacitors may be placed either between the driver and midbus, or between the midbus and

receiver, as long as both capacitors of a differential pair are placed in the same fashion. Other pairs within a link do not need to maintain this capacitor placement configuration.

Load Model

The Agilent Technologies load model for the midbus is given in the following figure. This model is subject to change. For the most current models, it is recommended that the platform designer contact Agilent Technologies directly.

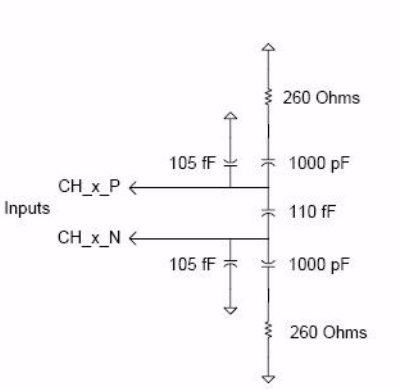


Figure 48 Load model for midbus probe

Reference Clock Probe

Both the midbus 2.0 (full size) probes and the N5328A half size midbus probe provide a reference clock probe for situations where it is necessary to probe a reference clock from the device under test (DUT).

For many solution setups, an external reference clock is not required. However, if any of the following cases are true, an external reference clock must be supplied for each PCI Express clock domain for which the case applies.

- When the midbus probe is used with a system that supports Spread Spectrum Clocking (SSC) on the reference clock to all the PCI Express agents and the SSC cannot be disabled
- When testing must be done with SSC enabled, because a problem does not manifest with SSC disabled.
- If the link frequency is intentionally margin tested outside the standard ±300 ppm tolerance.

NOTE

This is more restrictive than the PCI Express standard of ±300 ppm, but must be considered. For more information, contact Agilent Technologies directly.

The reference clock can be a dedicated clock, in which case appropriate terminators must be provided on the board. Alternately, the signals may be a tap off an existing clock, since the probes are designed to not significantly load the signals. Note that if the reference clock signal is series/source terminated then the position of the tap point must be at the far end of the line. However, this needs to be verified by the system platform designers to verify proper functionality. See reference clock model (Figure 19) for more information.

Mechanical Design Considerations for the Reference Clock Probe

A 3-pin header (1 by 3, 0.05 inch center spacing) will provide the connection for reference clock to the midbus. A small high impedance clock probe will connect to this header to the midbus. Note that an individual reference lock header is required for each PCI Express clock domain on the system.

The following are recommended part numbers for through-hole and surface mount versions of the 3-pin header for reference clock:

- Through- hole:

  Samtec* TMS- 103- 02- S- S
- Surface mount:

Samtec* FTR-103-02-S-S

Table 9 Reference clock header pinout

Signal	Pin Number
REFCLKp	1 (or 3)*
GND or N/C	2
REFCLKn	3 (or 1)*
* The probe can be plugged onto the pin header in either orientation.	

Reference Clock Probe Keep-Out Volume

Keep-out volumes for the reference clock probes are given in the following figure. The pin headers reside symmetrically within the keep-out volume on the target system. For more specific information on keep-out volumes for particular solutions please contact Agilent Technologies.

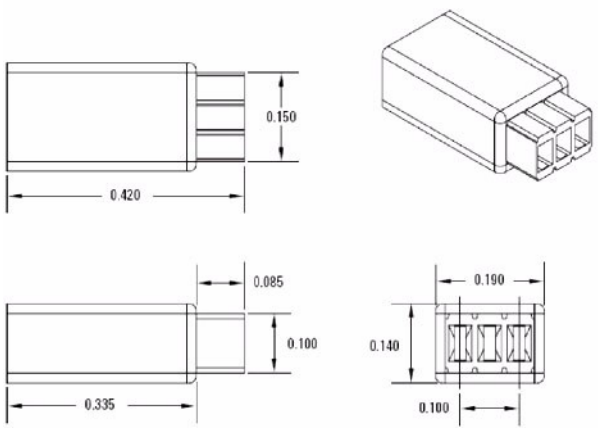


Figure 49 Reference clock probe keep-out volume

Electrical Design Considerations for the Reference Clock Probe

Table 10 Midbus reference clock electrical requirements

Midbus Requirement	Symbol	Min.	Max.	Comments
Differential voltage at ref clock attach point	Vppdiff	0.8 V	2 V	Vppdiff = |2*(Vrefclockp – Vrefclockn)|
Reference clock frequency without SSC	f	100 MHz -300 ppm	100 MHz +300 ppm	
Reference clock frequency with SSC	f	100 MHz -0.5%	100 MHz +0%	

If reference clock tolerance is less than ±300 ppm, there is no need for providing reference to the midbus. If the reference clock tolerance is greater than ±300 ppm, there is a need for providing reference (SSC) to the midbus.

Reference Clock Probe Load Model

Load models for the reference clock probe are given in this section. System designers will be expected to perform simulations of the reference clock networks with the header and midbus load models to ensure good signal integrity of the reference clocks at the header to the midbus. The pin header parasitics may be obtained from the connector vendor.

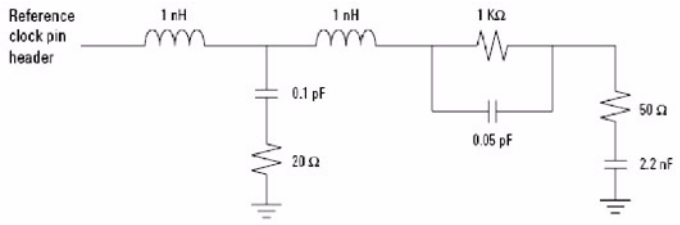


Figure 50 Reference clock probe load model

8 N4241F Flying Lead Probe

Resistor Dimensions 78
Lane Mapping 80
Important Points About Using N4241F 81

This chapter provides information on the N4241F flying lead probe used for PCIe.

WARNING **Do not directly touch any component on the N4241F flying lead cable set. It may be hot.**

CAUTION Components on the N4241F flying lead cable set are sensitive to the static electricity. Therefore, take necessary anti-static precautions, such as wear a grounded wrist strap, to minimize the possibility of electrostatic damage.

The *N4241F flying lead probe* is a probing solution for the N5306A I/O module, which you can use in situations where it is difficult to use midbus probes and solid slot interposer cards.

The N4241F flying lead probe allows probing of individual lanes, regardless of where they are routed. This eliminates the need to have signals routed to one probing point.

NOTE For information on solid slot interposer, refer to Chapter 5, "N5315 Solid Slot Interposer Card," starting on page 29.

For information on midbus probe, refer to *Agilent Soft Touch Midbus Probe 2.0, User's Guide*.

The following figure shows the N4241F flying lead cable set for x8 PCIe.

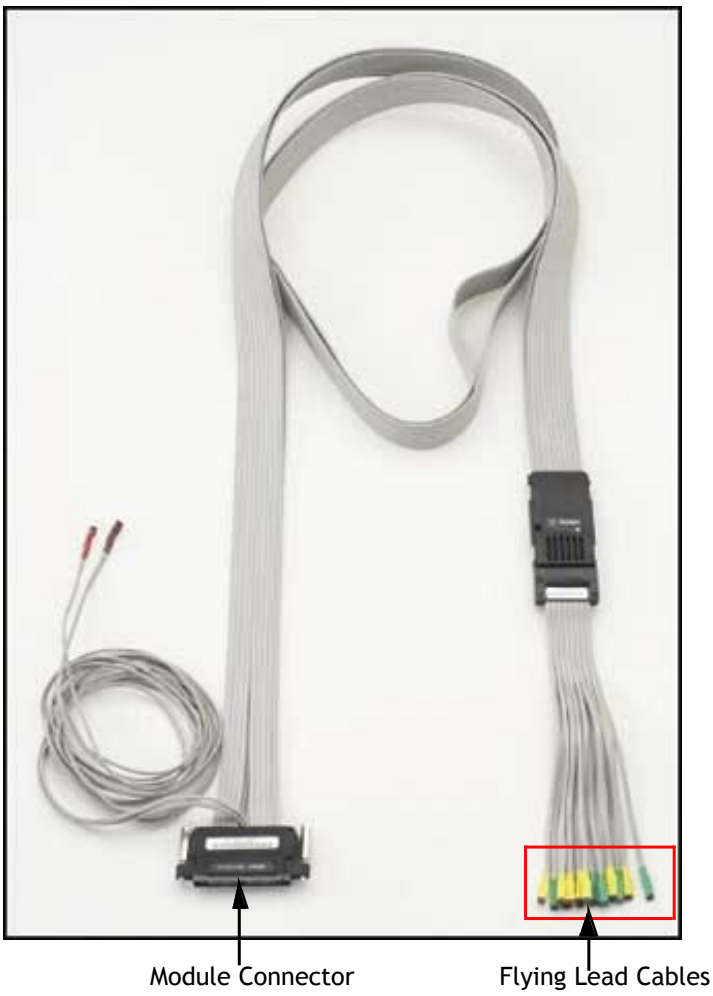


Figure 51 N4241F Flying Lead Probe

Components of the N4241F flying lead probe are described below:

- **Module Connector**— This component connects to the *Analyzer Probe* component of the N5306A I/O module.

  For information on N5306A I/O module, refer to Chapter 1, "N5306A I/O Module," starting on page 7.

- **Flying Lead Cables** flying lead cables— This component connects to DUT. There are 16 flying lead cables that you can use to connect to DUT via *resistors*.

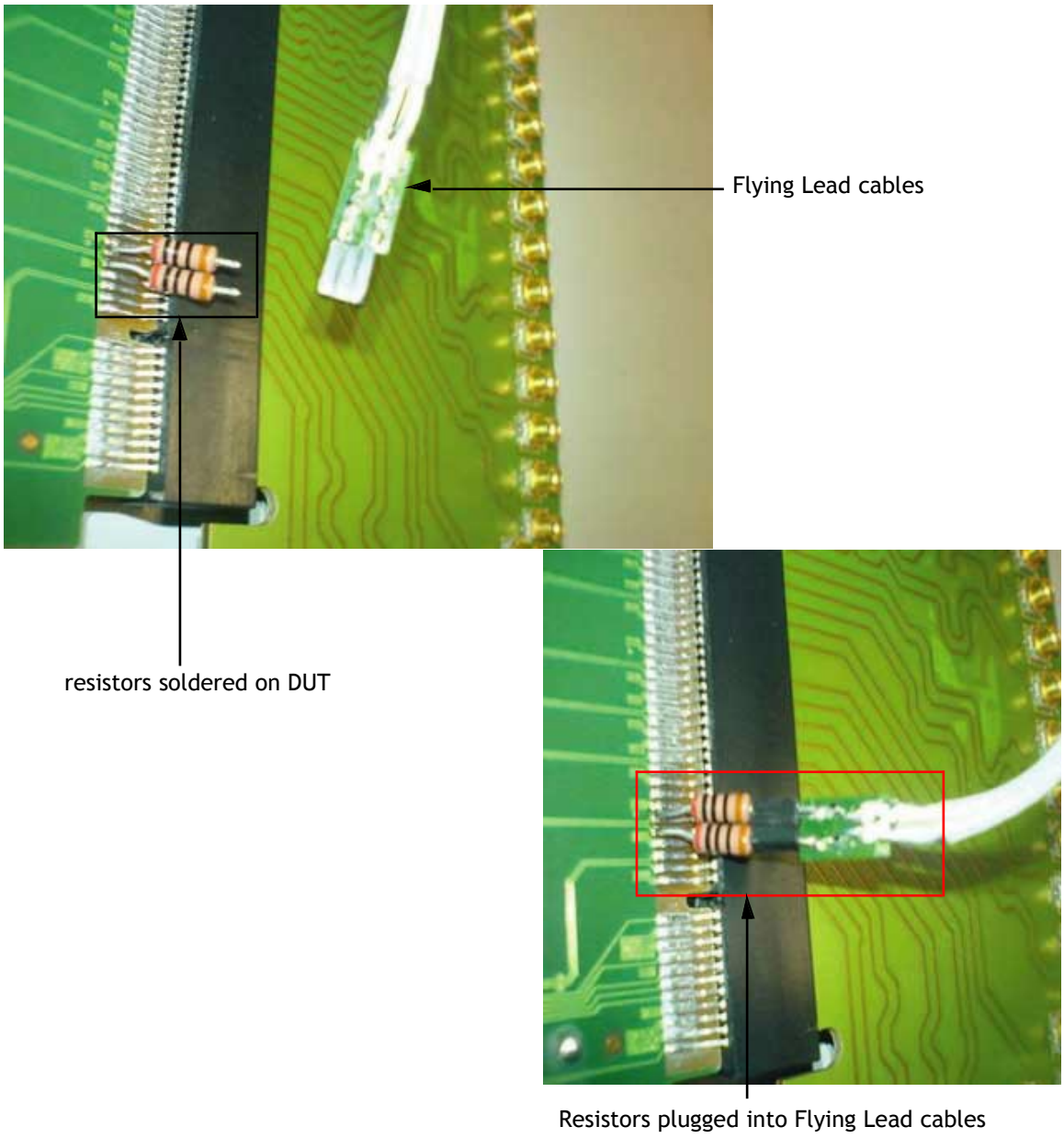


Figure 52 Flying Lead Cables using Resistors to connect with DUT

As shown in the figure above, the one end of resistors is first soldered onto DUT, and the other end is plugged into the flying lead cables.

NOTE

You can also solder resistors directly to the traces on the board. However, you should do this very carefully or these traces may get broken while soldering or releasing resistors.

Resistor Dimensions

The following figure shows the dimensions of the resistors (E5381-82101 Flying Leads Resistor Kit), that come with the flying lead cables.

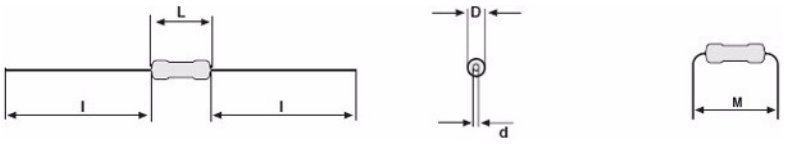


Figure 53 Dimensions of the resistors

NOTE You can purchase more resistor kits from Agilent Parts Direct using its part number.

The following table provides measurements of the resistor dimensions.

Table 11 Measurements of the resistor dimensions

Dimension Type	Measurement
Dmax.	1.6 mm
Lmax.	3.6 mm
dnom.	0.5 mm
lmin.	29.0 mm
Mmin.	5.0 mm
MASS	125 mg

As given in the table above, the diameter of the resistor ends (dnom.) is 0.5 mm. Therefore, the eye diameter on DUT, to which the one end of the resistor is soldered, should be 0.6 mm to properly hold the resistor. The other end of the resistor, which is plugged into the flying lead cables, should be short enough to avoid it from bending. Additionally, the distance between the eyes on a DUT should be large enough to avoid any contact between adjacently soldered resistors.

The diagram and the highlighted part in the following figure shows how you should be connecting resistors with eyes on DUT and flying lead cables.

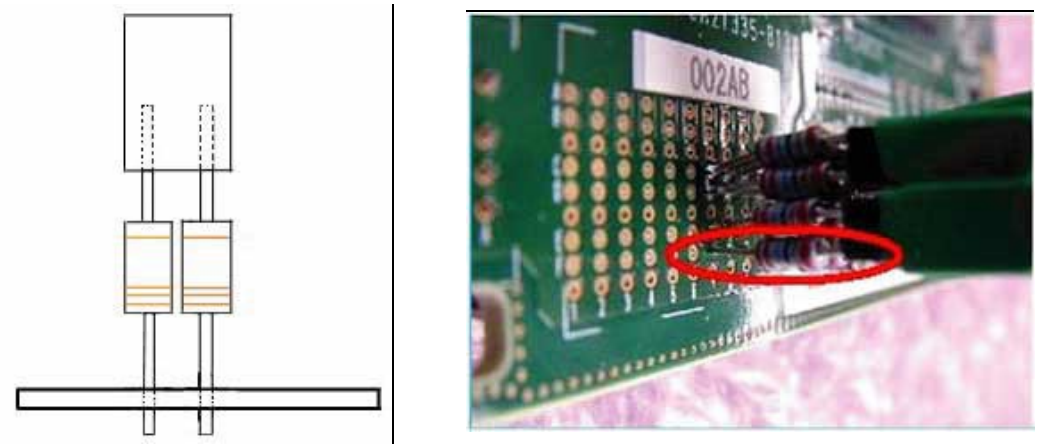


Figure 54 Resistors connecting with eyes and Flying Lead Cables

Lane Mapping

The following table provides the lane mapping information of the flying lead cables.

Table 12 Lane Mapping for N4241F Flying Lead Cables

Probe Label	x8 configuration with one N5306A module		x16 configuration with two N5306A modules
A0	upstream	Lane 0	Lane 0
A1	upstream	Lane 1	Lane 2
A2	upstream	Lane 2	Lane 4
A3	upstream	Lane 3	Lane 6
A4	upstream	Lane 4	Lane 8
A5	upstream	Lane 5	Lane 10
A6	upstream	Lane 6	Lane 12
A7	upstream	Lane 7	Lane 14
B0	downstream	Lane 8	Lane 1
B1	downstream	Lane 9	Lane 3
B2	downstream	Lane 10	Lane 5
B3	downstream	Lane 11	Lane 7
B4	downstream	Lane 12	Lane 9
B5	downstream	Lane 13	Lane 11
B6	downstream	Lane 14	Lane 13
B7	downstream	Lane 15	Lane 15

Important Points About Using N4241F

The following list provides more information about the N4241F flying lead probe:

- Its length is 60 inches (152.4 cm), and the length of its flying lead cables is 5.9 inches (15 cm).
- It supports 2.5 Gb/s and 5 Gb/s operation.
- It has input resistance of 297 Ohms.

  215 Ohms from internal tip resistor in series with 82 Ohms from external resistor.
- It allows probing of individual lanes, regardless of where they are routed. This eliminates the need to have signals routed to one probing point.
- It uses solder-on resistors for reference clock connections.
- Probe as close as possible to the receiver on the link.
- When soldering resistors, keep the channel side of the resistor as short as possible, as it will act as a stub and create reflection. However, the length of the probing resistors should match by +/-1 mm.
- Make sure that all resistors that are used to probe the channels on one direction of a PCIe link are placed in the same relative places. Symmetry between the two paired resistors is very important.

NOTE For more information on N4241F and its electrical characteristics, refer to the *Agilent E2960B Series for PCI Express 2.0* data sheet.

9 N4241Z ZIF Flying Lead Probe

N5426A ZIF Tip 86
N5451A Long Wired ZIF Tip 88
ZIF Flying Lead Connection to DUT 95
Lane Mapping 102
Important Points About Using N4241Z 103

This chapter provides information on the N4241Z ZIF flying lead probe used for PCIe.

The ZIF (Zero Insertion Force) flying lead system is a way to use a less expensive connection accessory (ZIF tip) that can be installed at many locations on a device under test, to connect to a flying lead (N4241Z) that transports the signal to the analyzer.

The advantages of this system are that the ZIF tip is very small and connects to the flying lead using a zero insertion force connector. The small size is critical when probing tight locations and the zero insertion force feature allows connection without compressing the delicate wires which cannot support this compression.

The Long Wired ZIF tip allows for a greater span between the two resistor wires.

WARNING **Do not directly touch any component on the N4241Z ZIF flying lead cable set. It may be hot.**

CAUTION Components on the N4241Z ZIF flying lead cable set are sensitive to the static electricity. Therefore, take necessary anti-static precautions, such as wear a grounded wrist strap, to minimize the possibility of electrostatic damage.

The *N4241Z ZIF flying lead probe* is a probing solution for the N5306A I/O module, which you can use in situations where it is difficult to use midbus probes and solid slot interposer cards.

The N4241Z ZIF flying lead probe allows probing of individual lanes, regardless of where they are routed. This eliminates the need to have signals routed to one probing point.

NOTE

For information on solid slot interposer, refer to Chapter 5, "N5315 Solid Slot Interposer Card," starting on page 29.

For information on midbus probe, refer to *Agilent Soft Touch Midbus Probe 2.0, User's Guide*.

The following figure shows the N4241Z ZIF flying lead cable set for x8 PCIe.

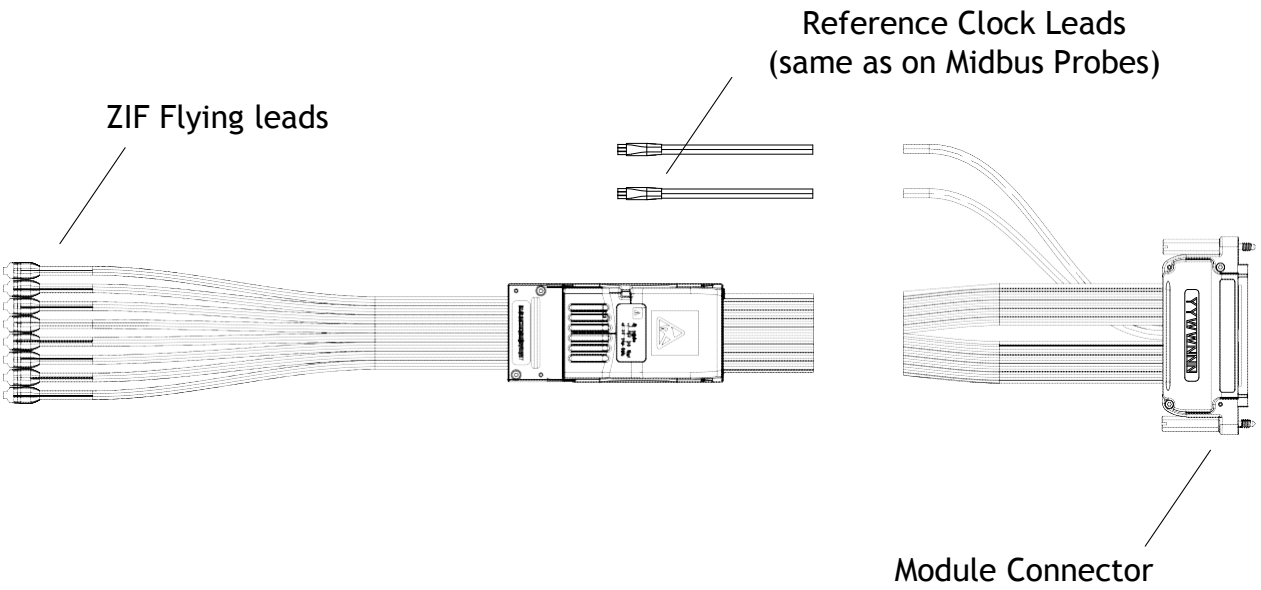


Figure 55 N4241Z ZIF Flying Lead Probe

The N4241Z ZIF flying lead probe has these components:

- **Module Connector**— This component connects to the *Analyzer Probe* component of the N5306A I/O module.

  For information on N5306A I/O module, refer to Chapter 1, "N5306A I/O Module," starting on page 7.

- **ZIF Flying Leads**— This component connects to DUT. There are 8 flying lead cables that you can use to connect to DUT via *ZIF tip boards*.

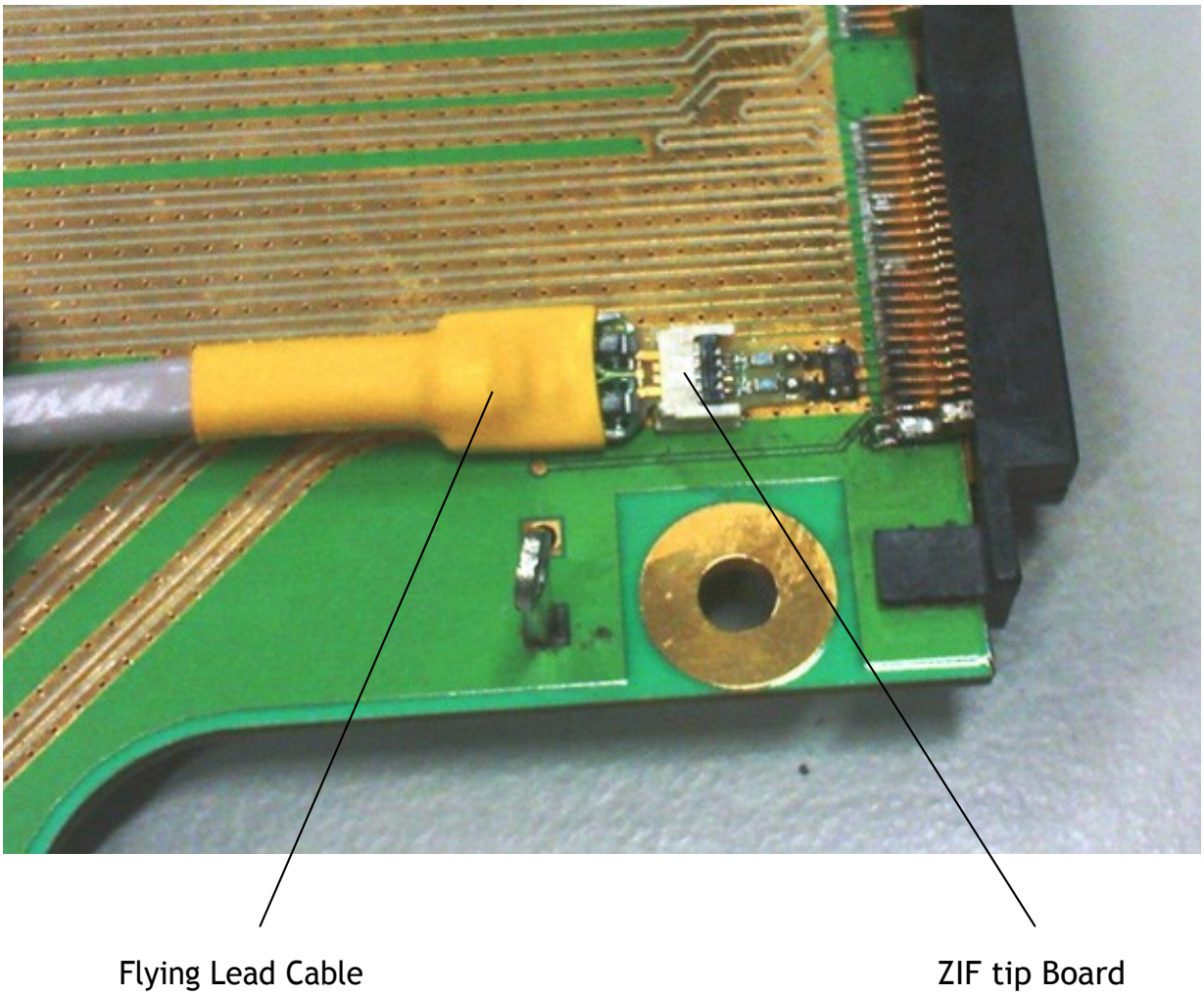


Figure 56 Flying Lead Cables using ZIF Tip Boards to connect with DUT

As shown in the previous figure, the ZIF tip board is first soldered onto DUT, and then the ZIF flying lead connects to the ZIF tip board.

N5426A ZIF Tip

This probe configuration provides the high bandwidth signals and the lowest capacitive loading for measuring both single-ended and differential signals.

The ZIF tip must be soldered to the circuit that you are measuring.

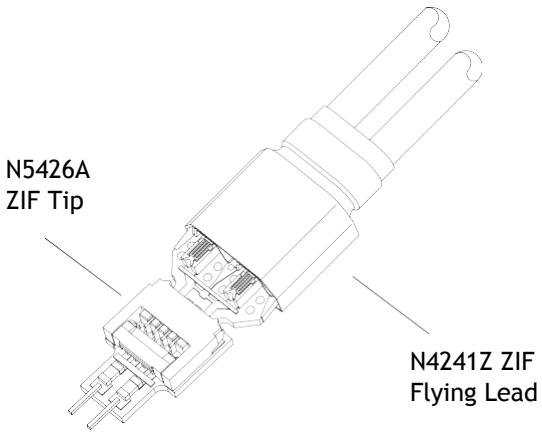


Figure 57 N5426A ZIF Tip

See Also

- "N5426A ZIF Tip Dimensions" on page 87

N5426A ZIF Tip Dimensions

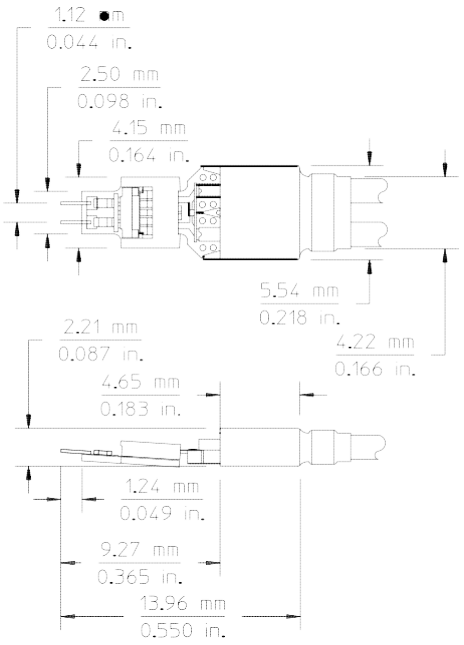


Figure 58 N5426A ZIF Tip Dimensions

N5451A Long Wired ZIF Tip

The Long Wired ZIF tip must be soldered to the circuit you are measuring. Use the shortest resistor length (7 mm or 11 mm) necessary for your application.

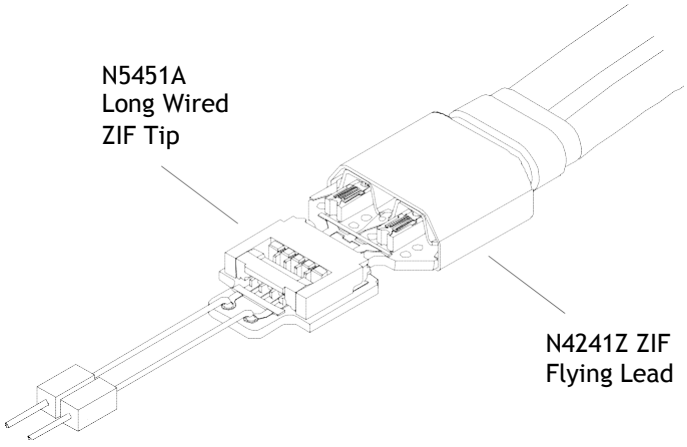


Figure 59 N5451A Long Wired ZIF Tip

Before using the resistor leads, they must be cut to the correct dimensions using the trim gauge and then soldered onto the Long Wired ZIF tip.

See Also

- "N5451A Long Wired ZIF Tip Dimensions" on page 89
- "Trimming Log Wired ZIF Tip Resistor Leads" on page 89
- "Soldering Resistors to Long Wired ZIF Tips" on page 91
- "Breaking Off Long Wired ZIF Tips from Packaging Strip" on page 94

N5451A Long Wired ZIF Tip Dimensions

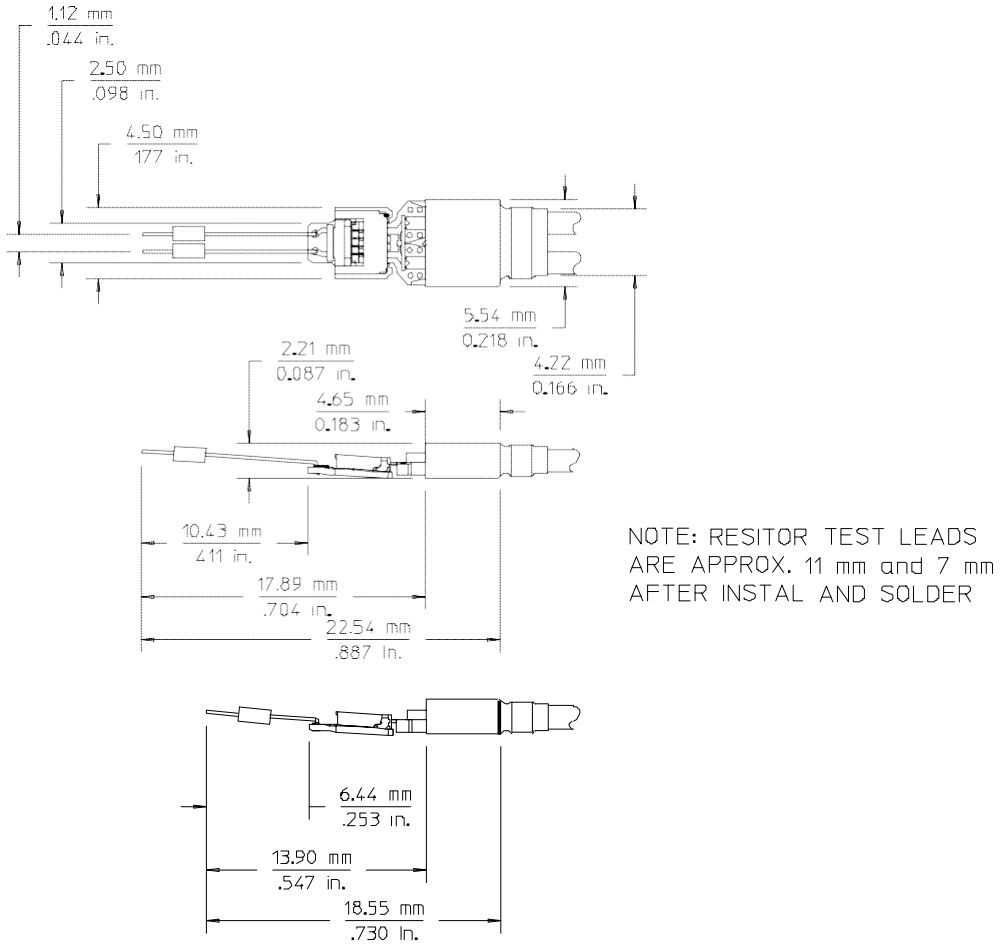


Figure 60 N5451A Long Wired ZIF Tip Dimensions

Trimming Log Wired ZIF Tip Resistor Leads

The following part number resistors must be trimmed and bent using the template (N5451A-94301) provided with the N5451A packaging:

- 01131-81510 (91 Ohm).

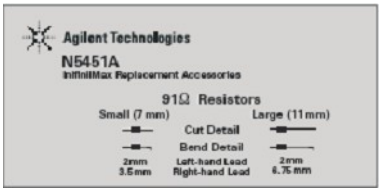


Figure 61 Template for Trimming Long Wired ZIF Resistor Leads

The template shows how to trim the leads to two different lengths: 7 mm or 11 mm. This equipment is required:

- X-acto knife.
- Agilent supplied template gauge (N5451A-94301) included as part of the N5451A packaging.
- Magnifying device.
- Tweezers (2).

The instructions for trimming and bending the resistor are:

1 Using tweezers, place the resistor body inside the rectangle of the trim template. The trim template contains two lengths: 7 mm and 11 mm. Choose the correct length for your application.

2 Using the X-acto knife, trim the leads even with the trim lines.

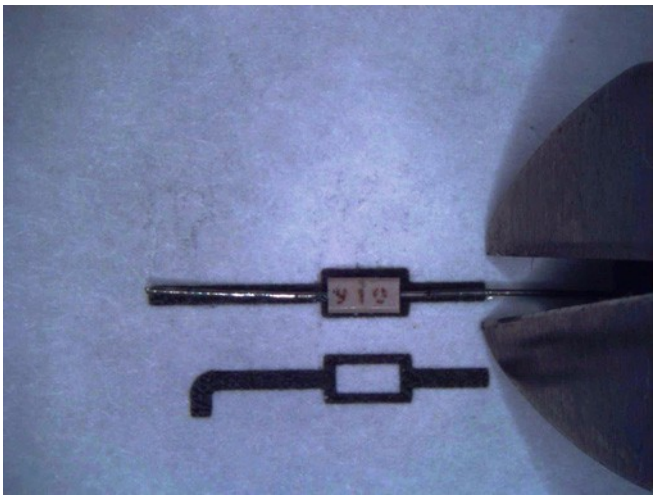
3 Place the resistor body inside the rectangle of the bend template.

4 Using another pair of tweezers, bend the right-hand lead 90 degrees.

For additional instructions and pictures regarding trimming, bending, and soldering these resistor leads, see "Soldering Resistors to Long Wired ZIF Tips" on page 91.

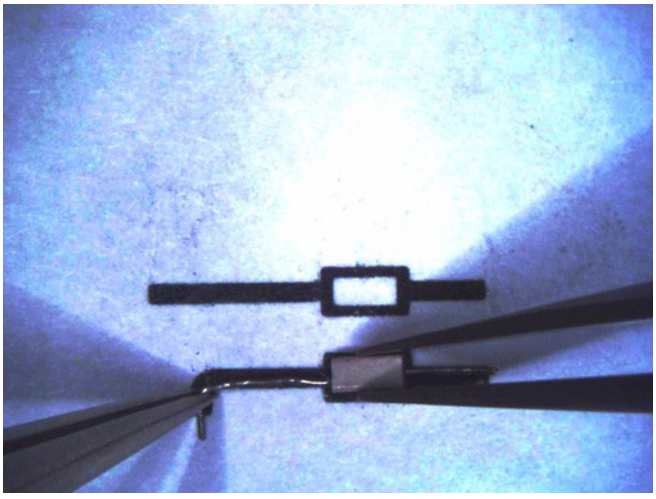
Soldering Resistors to Long Wired ZIF Tips

1 Choose a trim length of either 7 mm or 11 mm and use the corresponding trim guide dimensions to trim the resistor lead wires (see "Trimming Log Wired ZIF Tip Resistor Leads" on page 89).



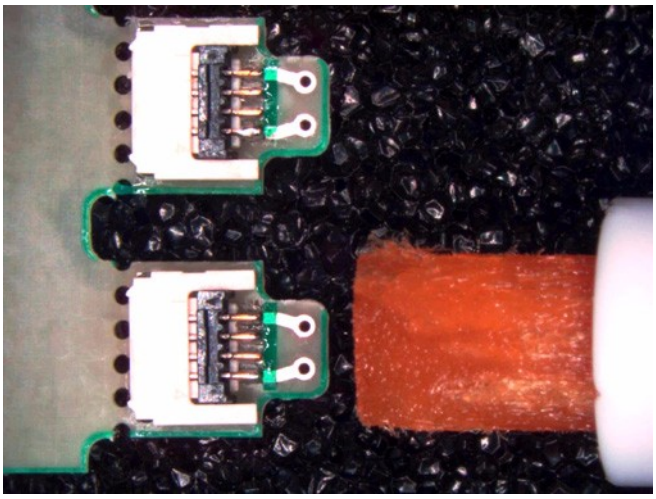
All measurements should be made from the corresponding resistor face datum. The included trim guide should be used for final length verification.

2 Bend the tip of the lead wire.

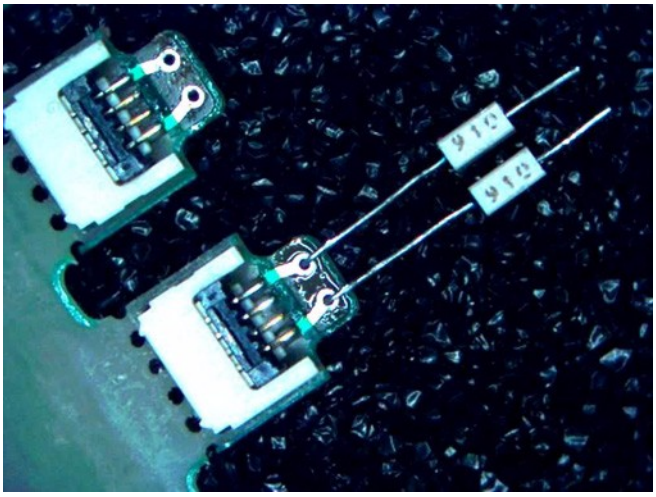


A sharp bend is preferred, but it should not exceed 90 degrees.

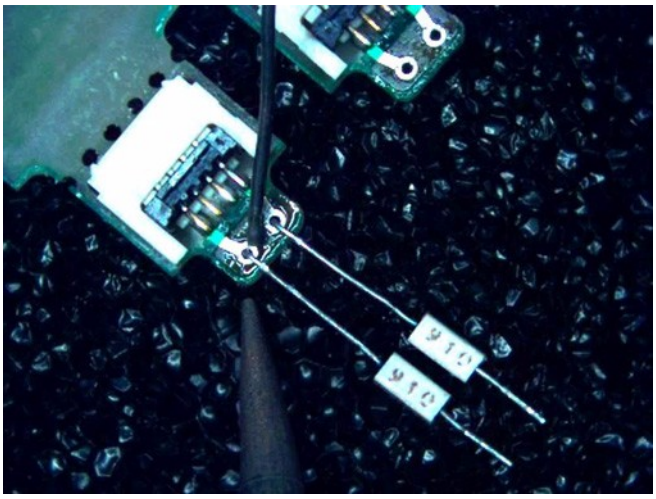
3 Use a flux pen to add flux to the circular traces on the board. The following figure shows a good application of flux.



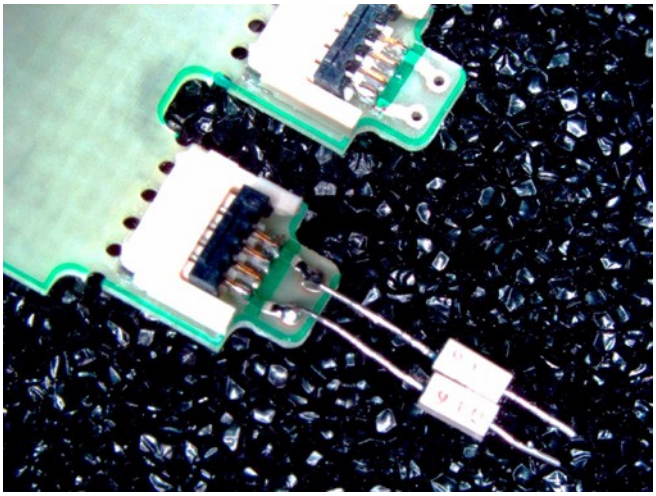
4 Insert one resistor into each through-hole of the circular traces on the board. Align the corresponding resistor faces. The following figure shows both the resistors installed and aligned. Make length adjustments as needed.



5 Momentarily apply the soldering iron tip to the resistor lead wires as shown the following figure.



Touch the solder to the heated lead wire near the trace hole. Now remove both the solder and the soldering iron away from the Long Wired ZIF Tip. A good fillet should form around the lead wire, thus sealing the trace hole. The following figure shows good solder fillets surrounding the resistor lead wires.

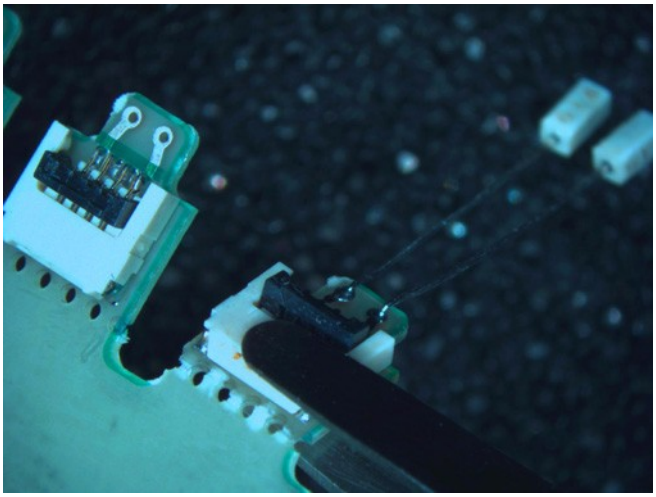


6 After soldering, clean board of any excess flux. Rotate the Long Wired ZIF Tip 180 degrees until the underside is facing up. Trim any excess lead wire protruding from the board.

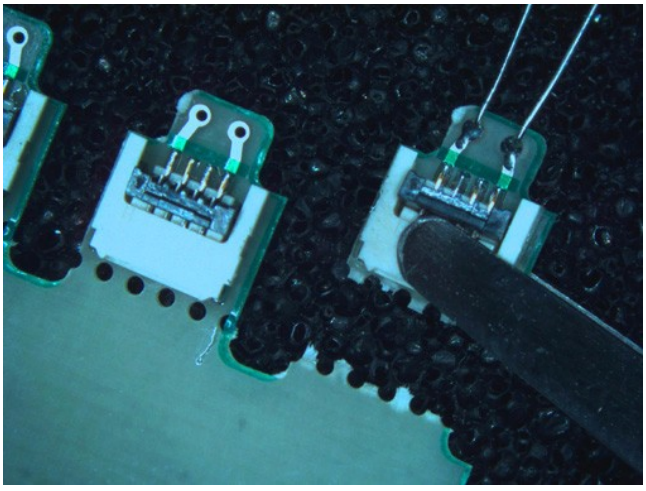
Breaking Off Long Wired ZIF Tips from Packaging Strip

The N5451A Long Wired ZIF tip kit contains ten ZIF tips connected together in a strip. Before a ZIF tip can be used, it must be separated from this strip of ten. To accomplish this:

1 Grab one of the tips with two fingers (or tweezers) and bend it back as shown in the following figure.



2 Then, bend the tip in the opposite direction and it should break off. The following figure shows what the tip looks like after it has been separated from the strip.



ZIF Flying Lead Connection to DUT

The pictures that follow show the N5426A ZIF tip. The Long Wired ZIF tip is soldered to the DUT in exactly the same manner.

- "ZIF Flying Lead Connection to DUT" on page 95
- "Soldering the ZIF Tip or Long Wired ZIF Tip into a DUT" on page 96

ZIF Tip Connection to Flying Lead

A close-up of the ZIF tip and the ZIF flying lead before the flying lead is inserted into the ZIF tip is shown in the following figure. Note that lever on the ZIF tip is shown in the open position (pointed up) which allows the insertion of the probe head contacts into the ZIF tip with zero insertion force.

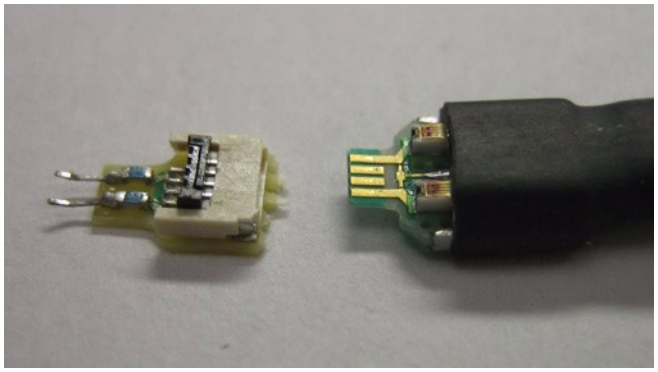


Figure 62 ZIF Tip (open position) and ZIF Flying Lead

A close-up of the ZIF flying lead inserted into the ZIF tip is shown in the following figure. Note that now the lever on the tip is in the closed position (down, rotated 90 degrees to the left) which closes the contacts of the ZIF connector.

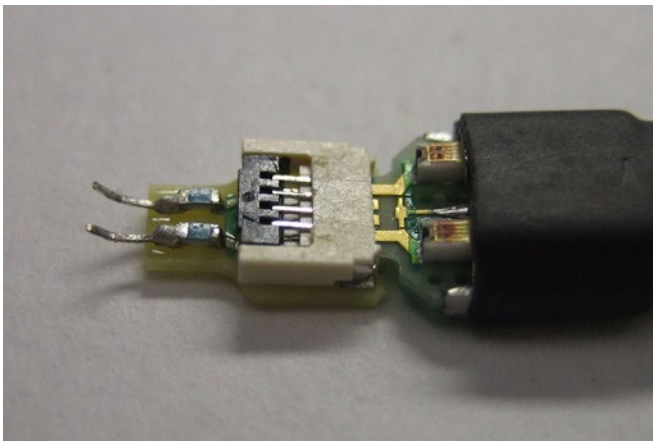


Figure 63 ZIF Tip (closed position) with ZIF Flying Lead Inserted

Soldering the ZIF Tip or Long Wired ZIF Tip into a DUT

Soldering the ZIF tip into a DUT is straightforward, but some of the traditional soldering techniques that are typically used on larger components will not work well here. Holding the leads on the ZIF tip in place while applying the soldering iron and adding solder requires the use of three hands.

This section shows an illustrated example of the installation of a ZIF tip and connection to a ZIF flying lead. The figures that follow show a ZIF tip being attached to the first two leads of an IC package. The ZIF tip could also be attached via pads or signal traces.

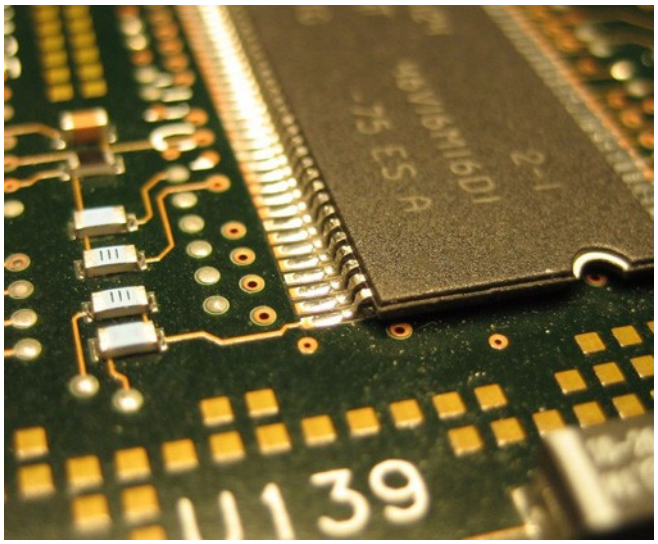


Figure 64 IC Package for Example ZIF Tip Installation

1 Add some solder to the target points in the DUT.

There should be enough solder to provide a good fillet around the ZIF tip leads, but not so much as to create a big solder ball. A fine MetCal (or equivalent) soldering tip should be used along with some 11 or 15 mil solder.

The following figure shows extra solder added to the pads for the first two pins on an IC package.

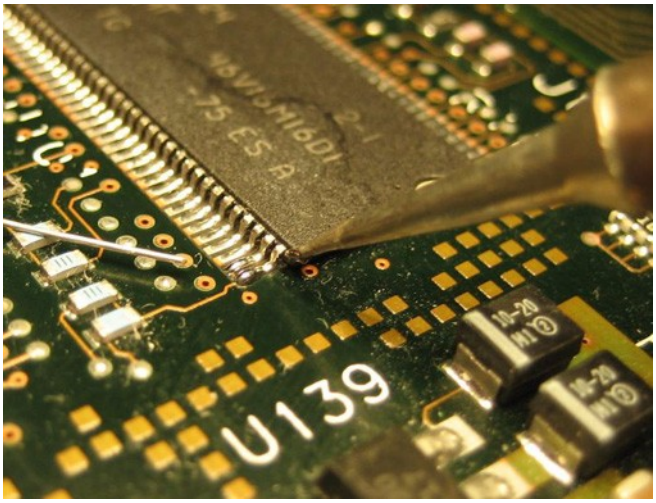


Figure 65 Solder Added to Target Points

2 Use a rosin flux pen to coat the solder points with flux.

The flux core solder does not provide enough flux for this small scale soldering.

Also, put flux on the tips of the leads of the ZIF tip.

The following figure shows the target points after they have been fluxed in preparation for soldering.

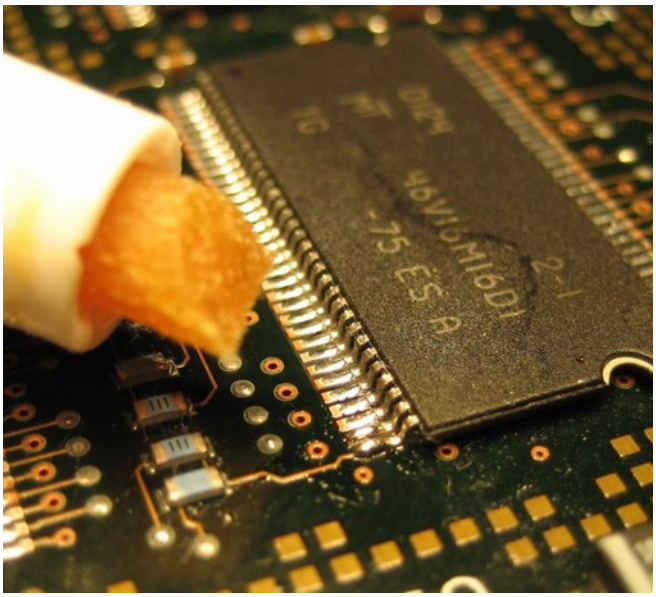


Figure 66 Fluxing of the Target Points

3 Clean the soldering iron tip, and add a small amount of solder to the very tip.

This may take a few tries because the solder may tend to ball up and move away from the tip.

The solder on the tip keeps the soldering iron tip from pulling solder off the DUT connection points.

This step may be optional if there is already enough solder on the DUT connection points.

The following figure shows a small amount of solder on the tip of the soldering iron.

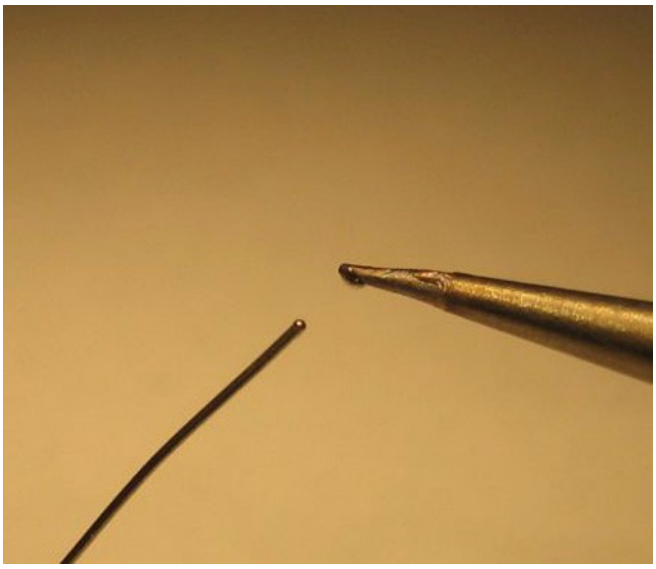


Figure 67 Small Amount of Solder Added to ZIF Tip of Soldering Iron

4 Installation of ZIF tip. Connect the ZIF tip to the ZIF flying lead as shown in "ZIF Flying Lead Connection to DUT" on page 95. This allows the flying lead to be used as a handle for the ZIF tip to allow positioning in the DUT.

Position a lead of the ZIF tip on top of one of the target points, then briefly touch the soldering iron tip to the joint. The thermal mass of this joint is very small, so you don't need to dwell on the joint for very long.

There should be enough solder to form a good fillet and enough flux to make the joint shiny. There should not be so much solder such that a big solder ball is formed that could cause a solder bridge or cause a flow that overheats the leads on the ZIF tip, causing the leads to come off and destroying the tip. Only the first third of the lead or so needs to be soldered to the target point.

If you do not get a good, shiny, strong solder joint, there was either not enough flux or the joint was heated too long and the flux boiled off.

The following figure shows the ZIF tip leads soldered in place.

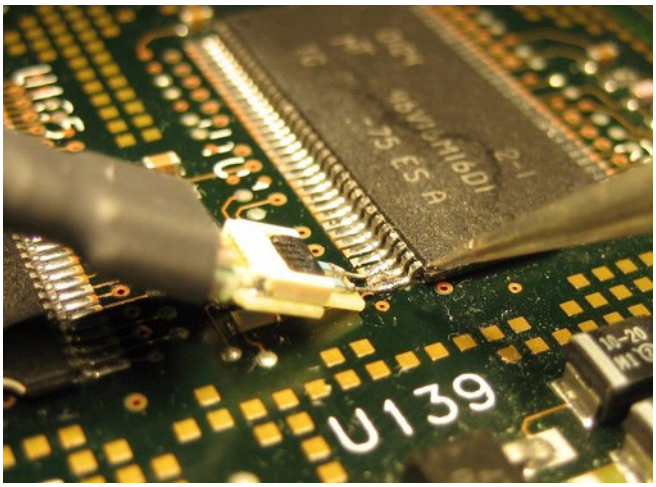


Figure 68 ZIF Tip Positioned and Soldered In Place

5 Remove ZIF flying lead and leave ZIF tip behind for future connection. It is best to use a non-conductive, pointed object such as a tooth pick or plastic tool. Hold on the heat-shrink part of the probe head to support the ZIF Tip while releasing the latch.

The following figure shows a toothpick releasing the latch on the ZIF connector.

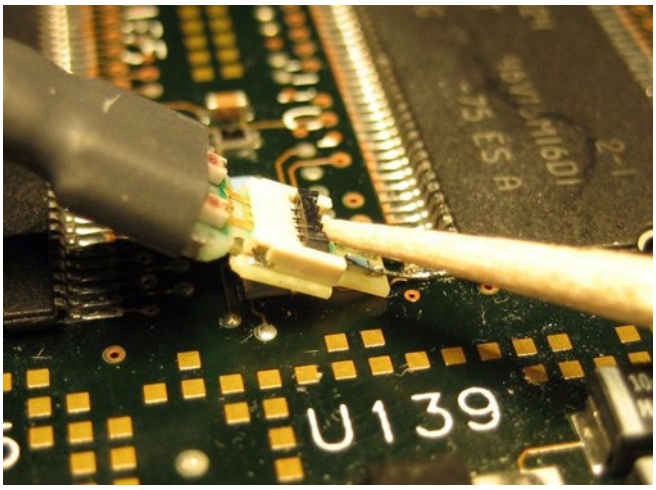


Figure 69 Using a Non-conductive Tool to Open the ZIF Connector

The following figure shows the ZIF tip left behind in the DUT with the latch open, ready for future connections.

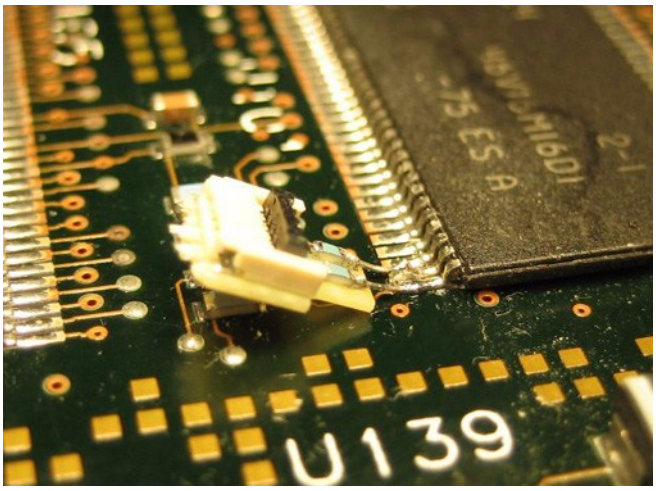


Figure 70 ZIF Tip Left Behind in DUT with ZIF Latch Open

6 Connect the ZIF flying lead to the ZIF tip desired for measurement.

When you need to make a measurement at a point where you have previously installed a ZIF tip, ensure the latch on the ZIF tip is open, insert the contacts on the flying lead into the ZIF socket, and then close the ZIF latch with a non-conductive tool.

Depending on the positioning of the ZIF tip, you may need to support the body of the ZIF tip while closing the latch. This can be done with tweezers or other another suitable tool by grabbing the PC board at the tip while the latch is being closed. If the circuit is live and there is concern about shorting anything out, use plastic or non-conductive tweezers. See the following figure.

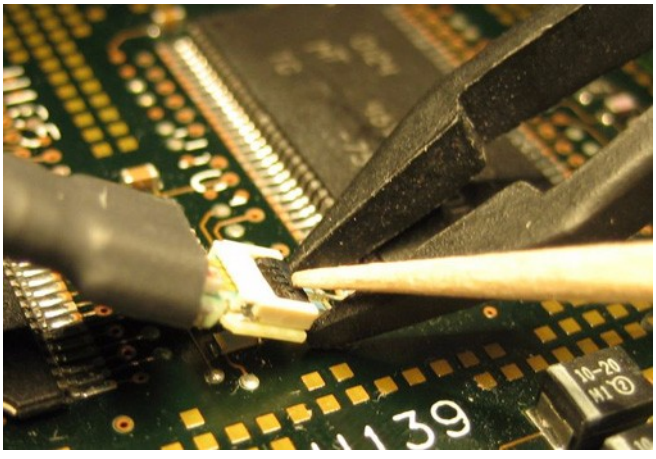


Figure 71 Use a Non-conductive Tool to Close the Latch

Lane Mapping

The following table provides the lane mapping information of the flying lead cables.

Table 13 Lane Mapping for N4241Z ZIF Flying Lead Cables

Probe Label	x8 configuration with one N5306A module		x16 configuration with two N5306A modules
A0	upstream	Lane 0	Lane 0
A1	upstream	Lane 1	Lane 2
A2	upstream	Lane 2	Lane 4
A3	upstream	Lane 3	Lane 6
A4	upstream	Lane 4	Lane 8
A5	upstream	Lane 5	Lane 10
A6	upstream	Lane 6	Lane 12
A7	upstream	Lane 7	Lane 14
B0	downstream	Lane 8	Lane 1
B1	downstream	Lane 9	Lane 3
B2	downstream	Lane 10	Lane 5
B3	downstream	Lane 11	Lane 7
B4	downstream	Lane 12	Lane 9
B5	downstream	Lane 13	Lane 11
B6	downstream	Lane 14	Lane 13
B7	downstream	Lane 15	Lane 15

Important Points About Using N4241Z

The following list provides more information about the N4241Z ZIF flying lead probe:

- Its length is 60 inches (152.4 cm), and the length of its flying lead cables is 7.9 inches (20 cm).
- It supports 2.5 Gb/s and 5 Gb/s operation.
- It has input resistance of 282 Ohms.

  200 Ohms from internal tip resistor in series with 82 Ohms from ZIF tip.
- It is supplied with the N5426A (standard) or N5451A (long wired) ZIF tip kits.
- It allows probing of individual lanes, regardless of where they are routed. This eliminates the need to have signals routed to one probing point.
- It uses ZIF tip boards for reference clock connections.
- Probe as close as possible to the receiver on the link.

  See the *User's Guide* for the ZIF kit attachment.

NOTE For more information on N4241Z and its electrical characteristics, refer to the *Agilent E2960B Series for PCI Express 2.0* data sheet.

9 N4241Z ZIF Flying Lead Probe

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